

MS-7B84 Ver:1.0

CPU:

AMD AM4

System Chipset:

Promontory A320 & B350 & B450
(Value DIY or System Builder)

Main Memory:

DDR IV * 2 MAX:32 GB

VRM

RT8894 4+2

On Board Chipset:

LPC Super I/O --NCT5567

LAN RTL8111H

Azalia CODEC - Realtek ALC887

Expansion Slots:

From CPU

PCI Express X16 Slot * 1

PCI Express X1 Slot * 1

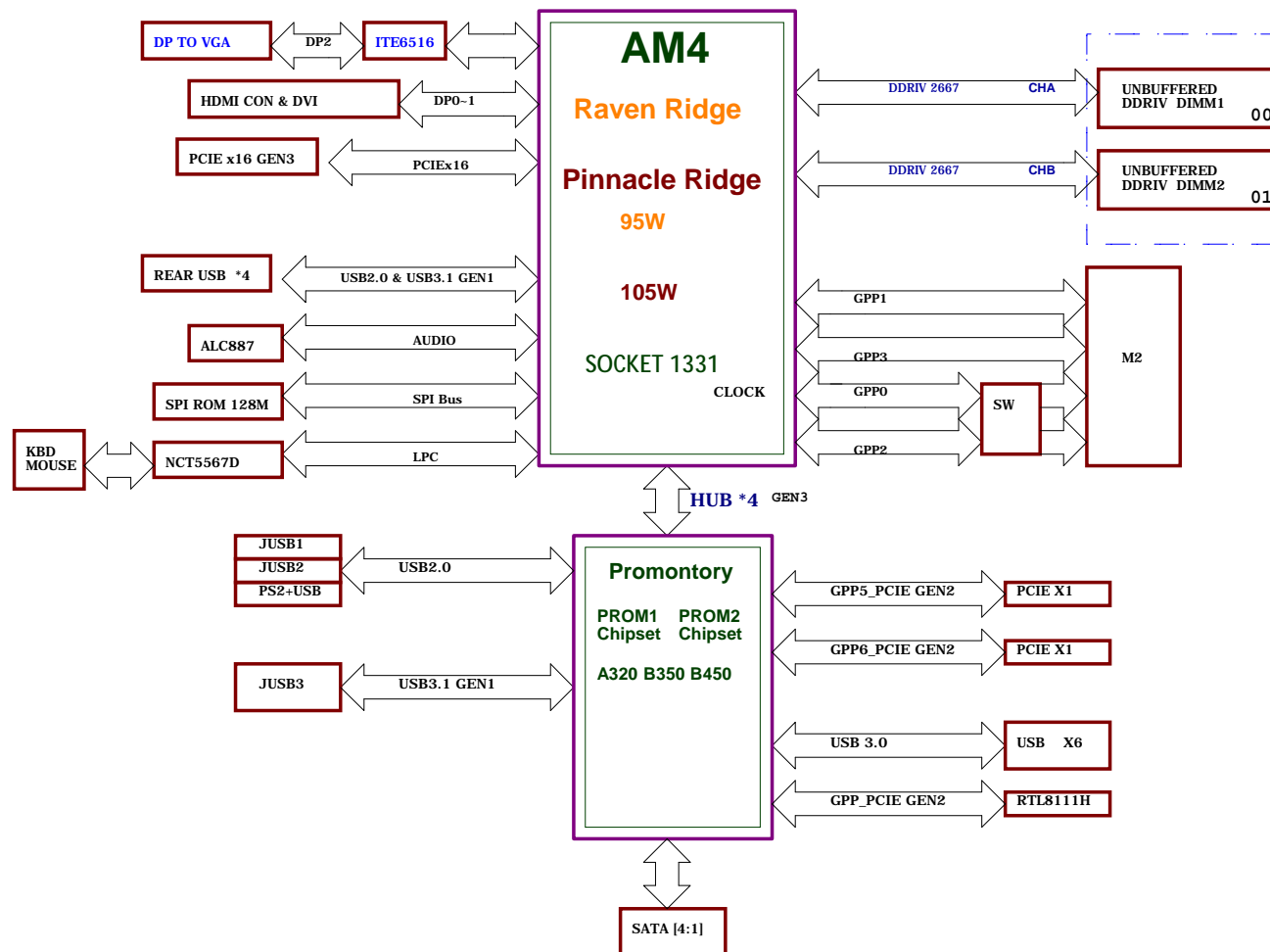
PCI Express X1 Slot * 1

M2_2 * 1

OCP IC:

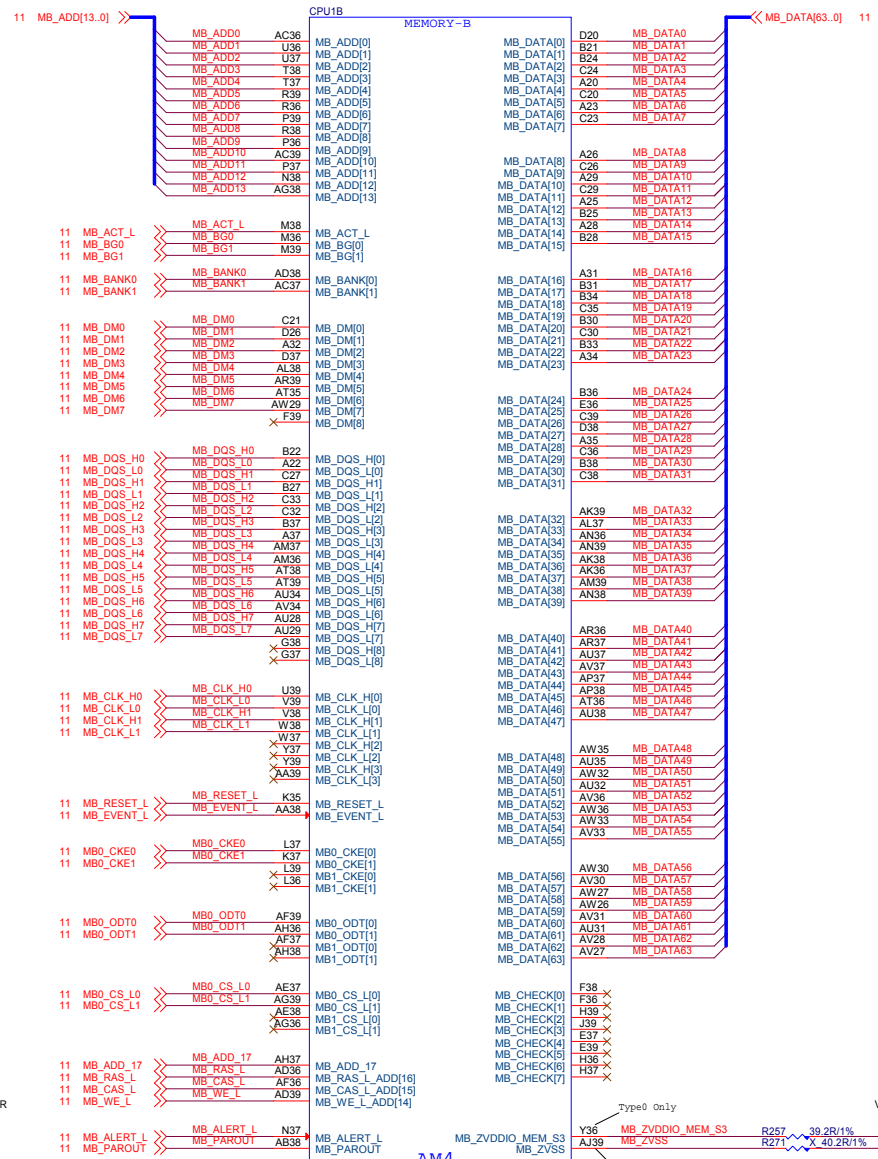
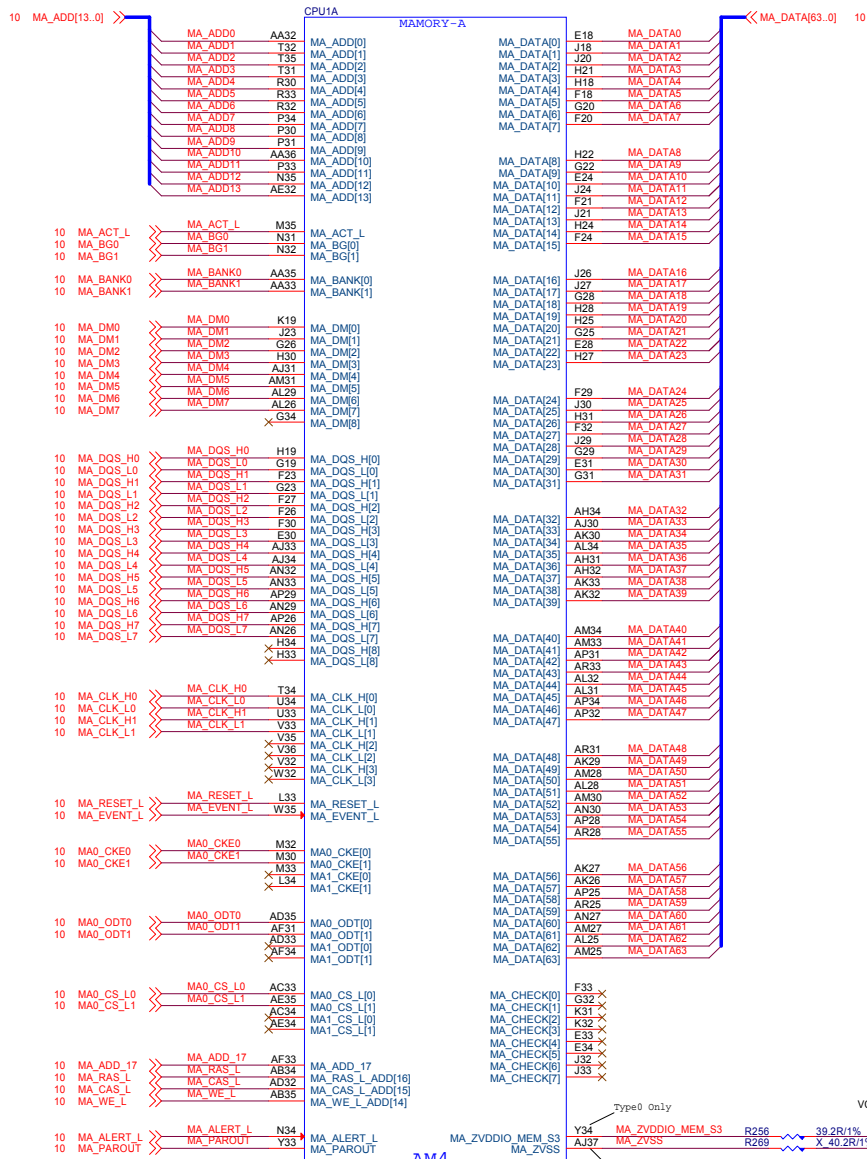
RT9553B

FUSION BLOCK DIAGRAM



AMD AM4

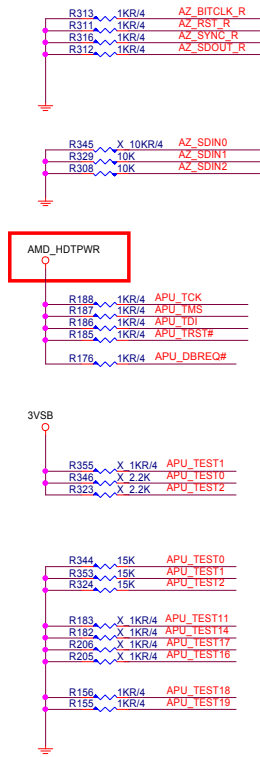
01 Block Diagram	37 CPU Power VDDP-MP8712
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03 FM4 DDR4 I/F	39 CPU Power RT8894 3+2 Phase
04 AM4 PCIE/SATAE	40/41 CPU Power Phase 1-4
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28 USB Front Side	
29 SATA Connector	
30 HDMI Connector	
31 DP to VGA RTD2166	
32 ACPI uPI-5VDIMM&3VSB	
33 PM-SY8288RAC-1.05V/GS7133-2.5V	
34 DDR PWR VPP25/VTT-MP2147	
35 DDR Power-RT8231AGQW	
36 CPU Power 1P8V-MP2147	



Schematic Cfg

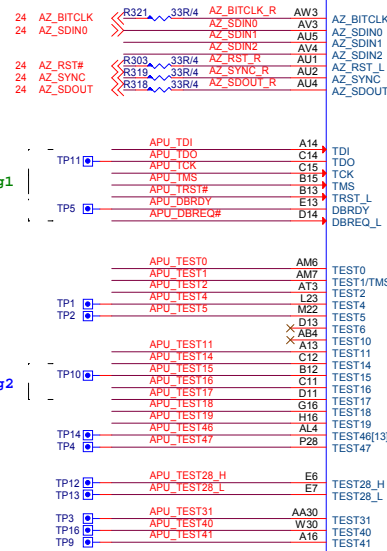
Project

V A



For Debug1

For Debug2



AM4
PART 4 OF 9

ZIF-SOCKET1331-HF

DVI change to HDMI



For HDMI

For DVI

Not supported on TYPE 2

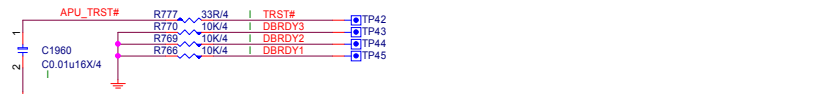
AM4 Type 1 processors: DP2 is not supported
50724 1_13

RV2 AM4 35W is a de-featured version
of RV1 AM4 65W, RV2 AM4 35W
can only support 2 displays

Here is the example of Raven2 AM4's DP2 function on existing AM4 board :
1.D-sub : DP to VGA translator (e.g. ANX62xx) ok
2.DP : only 2 lanes can work (lane 0 and lane1)
3.DVI-D : no display (no TMDS clock on lane3)
4.HDMI : no display (no TMDS clock on lane3)
by mail 2017-11-28

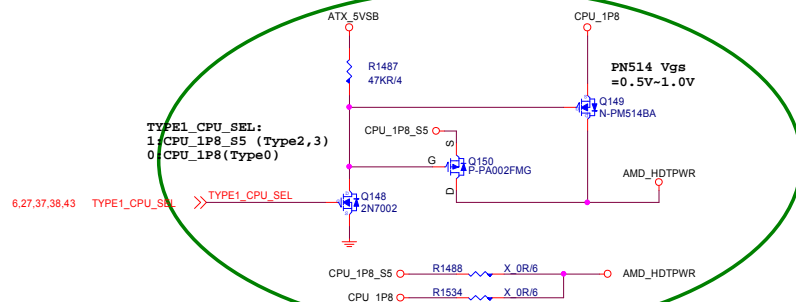
Not support Type2

K14 PIN: 不管SPEC有沒有HDMI,都需PU HIGH,
這樣使用DVI轉HDMI Dongle,接上HDMI螢幕才會有聲音輸出



Stuff for first model

11-15



$$IB = (AMD_HDTPWR - Vbe) / 4.7k$$

$$(1.8 - 0.95) / 4.7k = 0.181mA$$

$$IC = (Vc - Vce) / 10k$$

$$(1.8 - 0.2) / 10k = 0.16mA$$

$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

$$IB = (Vb - Vbe) / 10k$$

$$(1.75 - 0.95) / 10k = 0.08mA$$

$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

$$IC = (Vc - Vce) / 10k$$

$$(3.3 - 0.2) / 10k = 0.16mA$$

$$IB = (AMD_HDTPWR - Vbe) / 4.7k$$

$$(1.8 - 0.95) / 4.7k = 0.181mA$$

$$IC = (Vc - Vce) / 10k$$

$$(1.8 - 0.2) / 10k = 0.16mA$$

$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

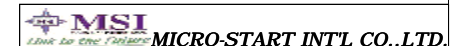
$$IB = (Vb - Vbe) / 10k$$

$$(1.75 - 0.95) / 10k = 0.08mA$$

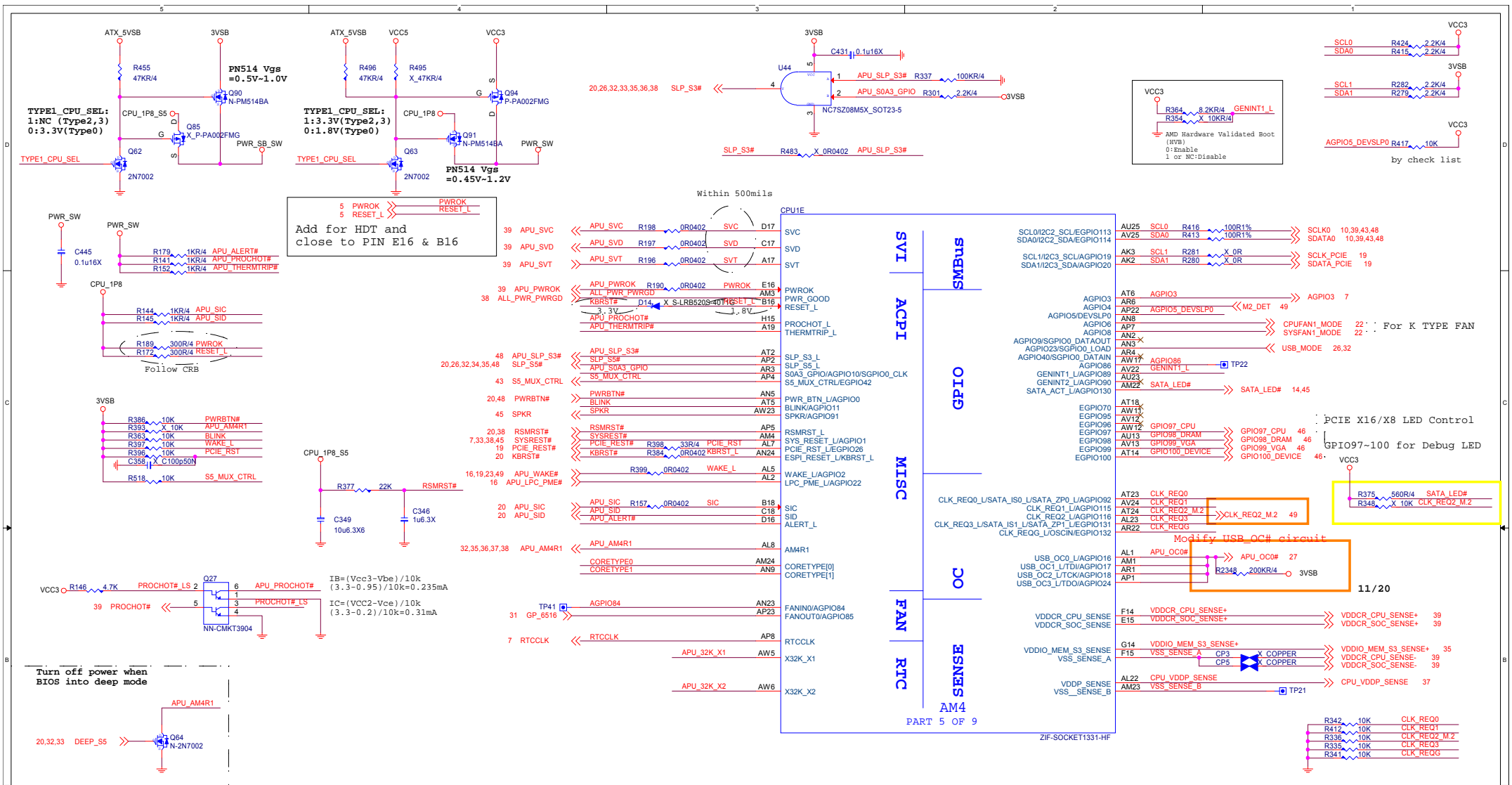
$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

$$IC = (Vc - Vce) / 10k$$

$$(3.3 - 0.2) / 10k = 0.16mA$$

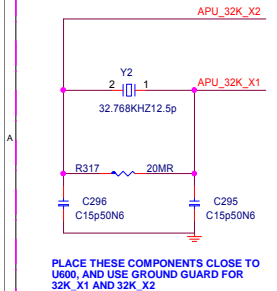


AM4 DISPLAY/AUDIO		
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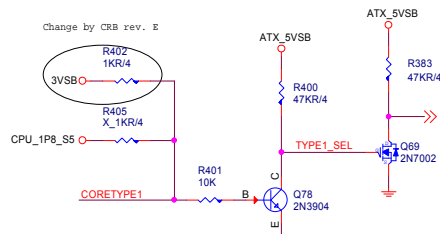


Layout: Place x'tal within 1.5 inch of APU

AM4 CPU TYPE Circuit



Change by CRB rev. B

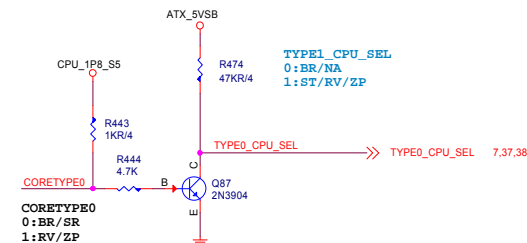


CPU	TYPE	CORETYPE	0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1

TYPE1_CPU_SEL
0: BR/NA
1: ST/RV/ZP

**IB=(Vcc3-Vbe)/21k
(3.3-0.95)/21k=0.111mA**

**IC=(VCC5-Vce)/10k
(5-0.2)/47k=0.102mA**



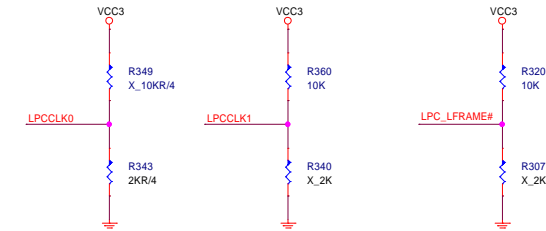
**IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA**

**IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA**

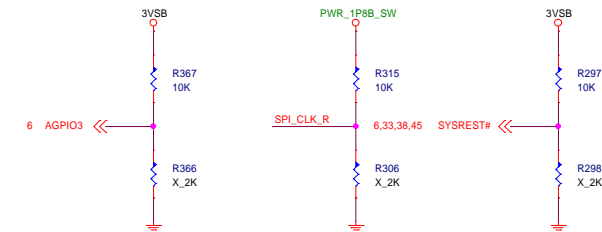
MSI
MICRO-START INTL CO., LTD.

File	Document Number	Rev
AM4 SVI/ACPI/GPIO	MS-7B84	1.0
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Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM (Default)

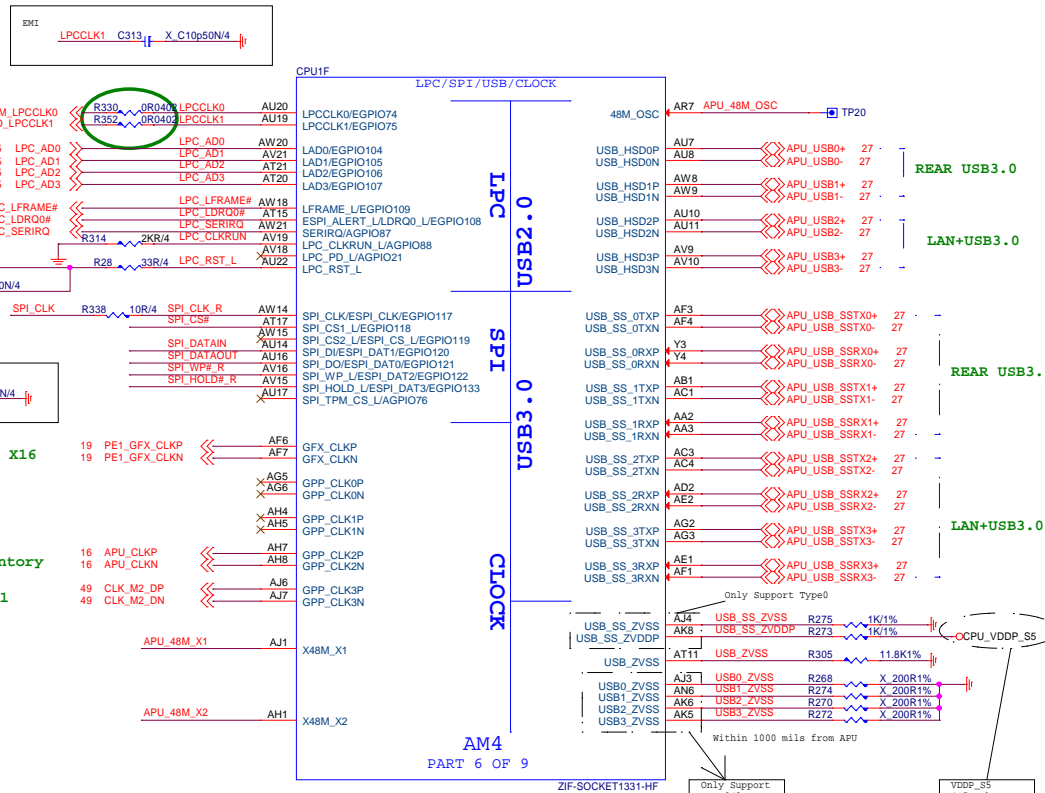


	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

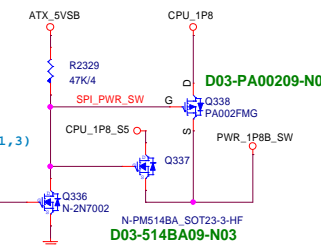
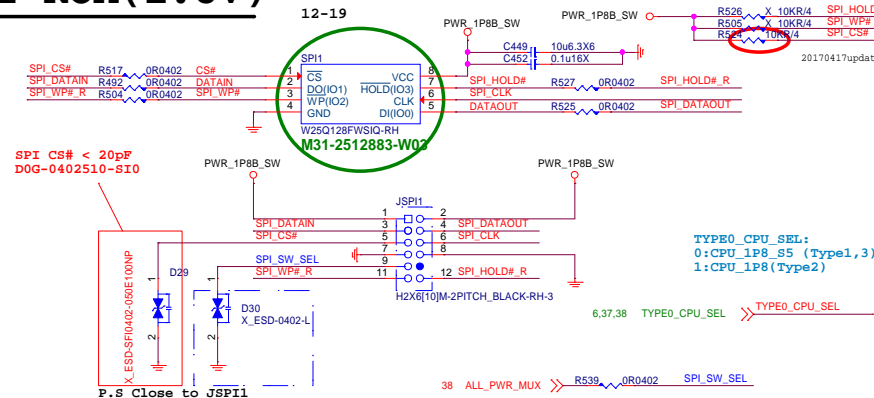
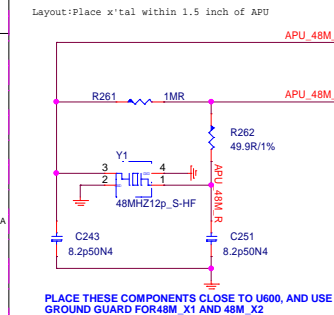
	RTCCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

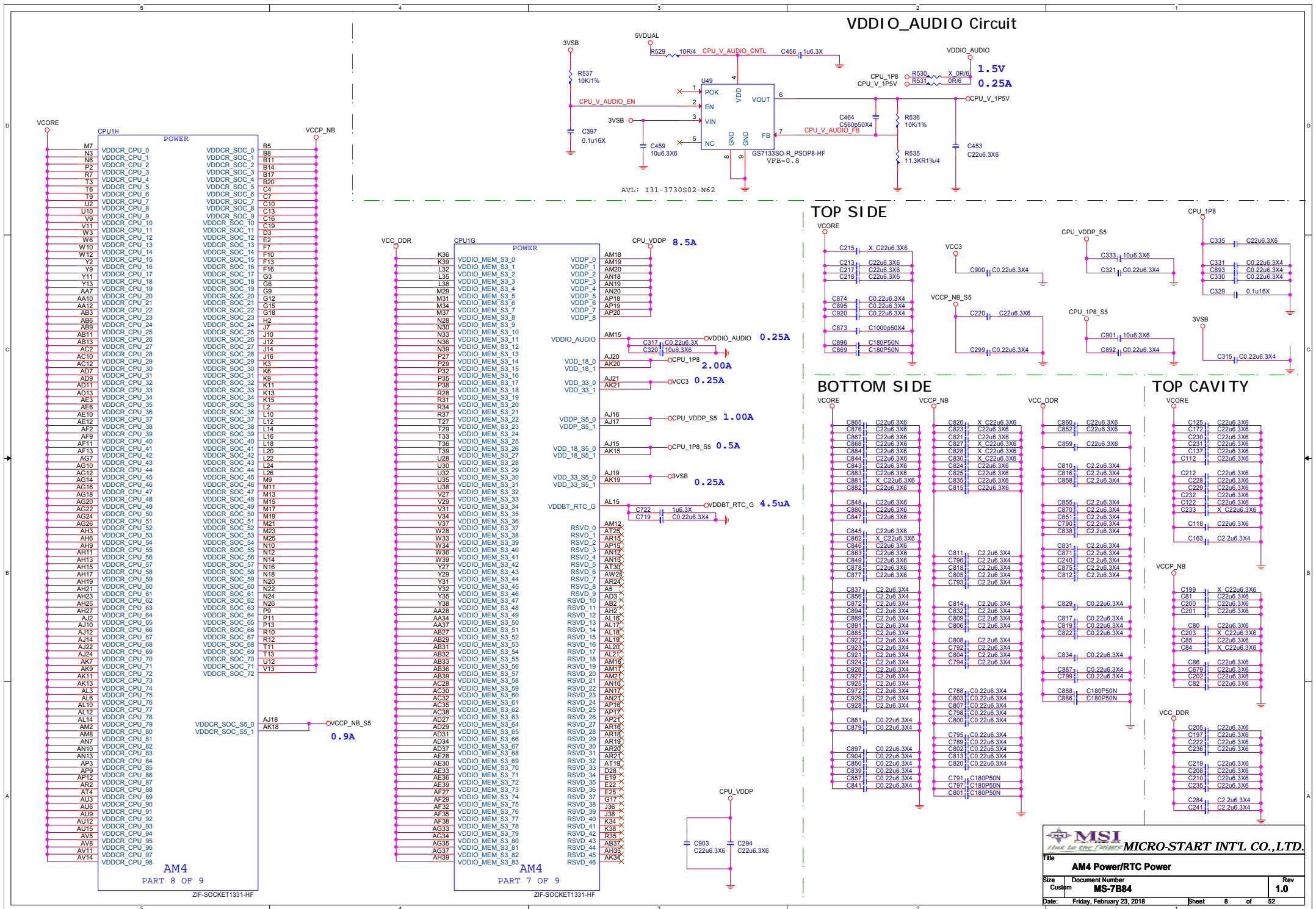
MSI
MICRO-START INTL CO.,LTD.

File	AM4 LPC/SPI/USB/CLK/STRAP	Rev	1.0
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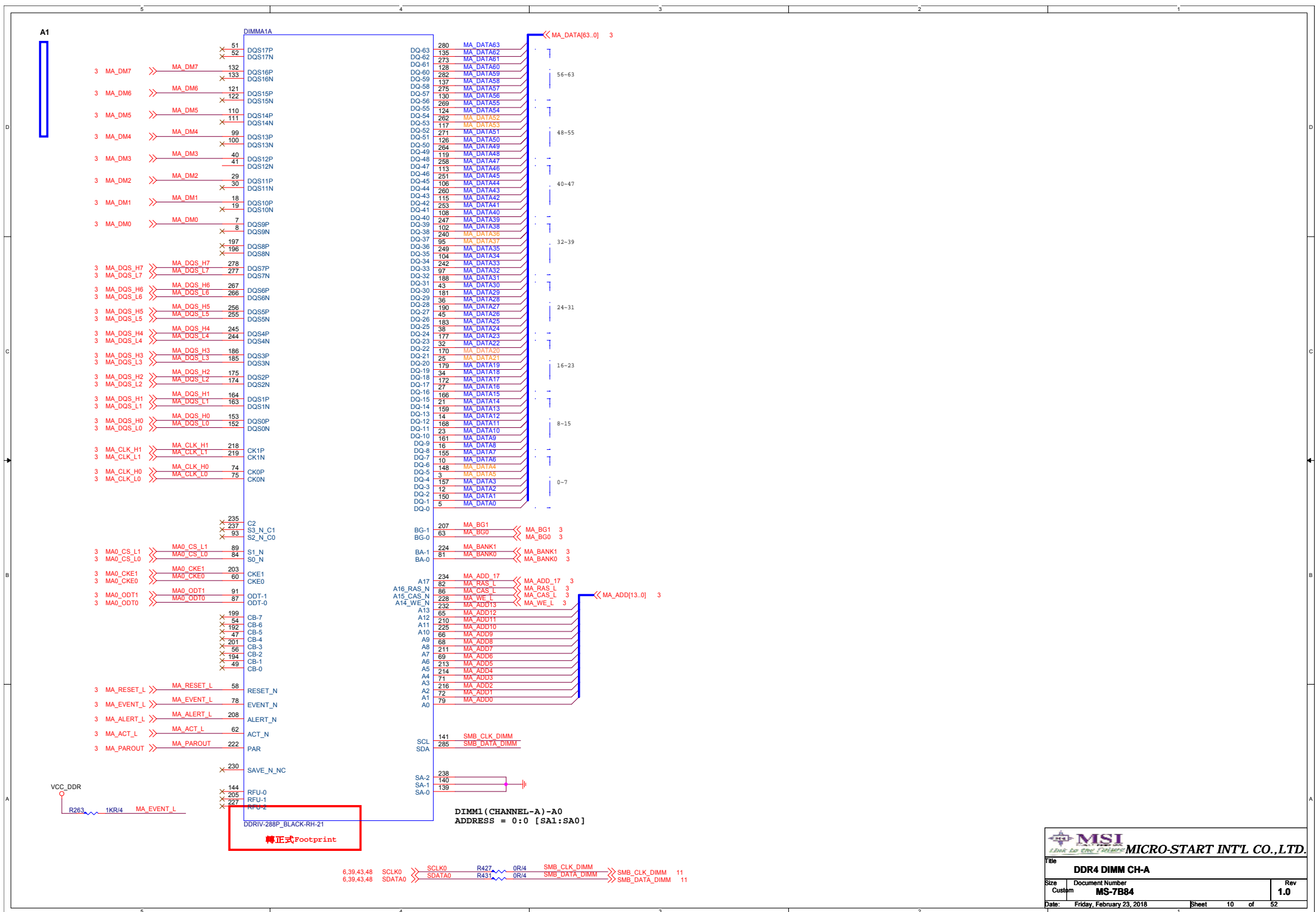
SPI ROM(1.8V)

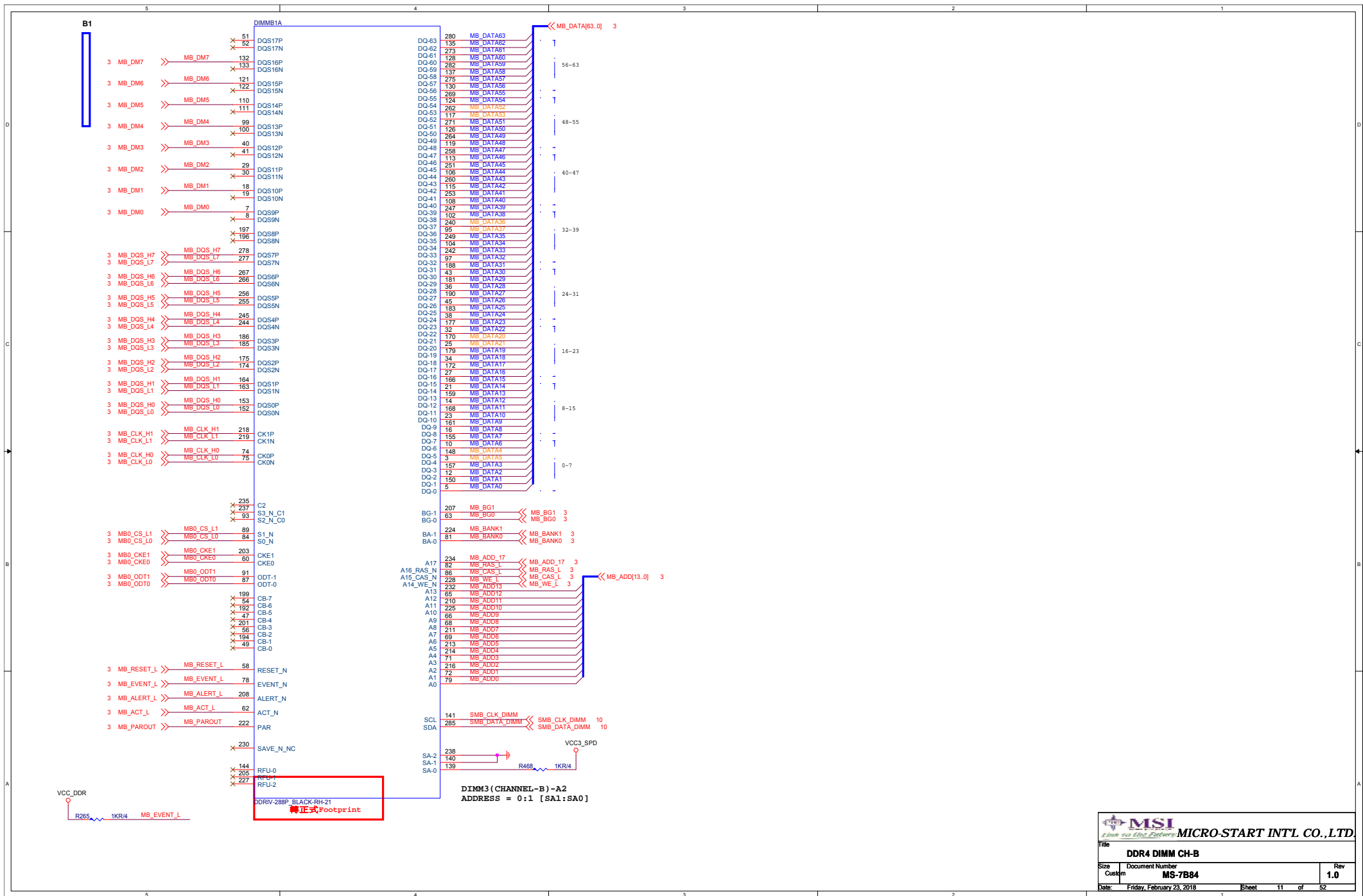


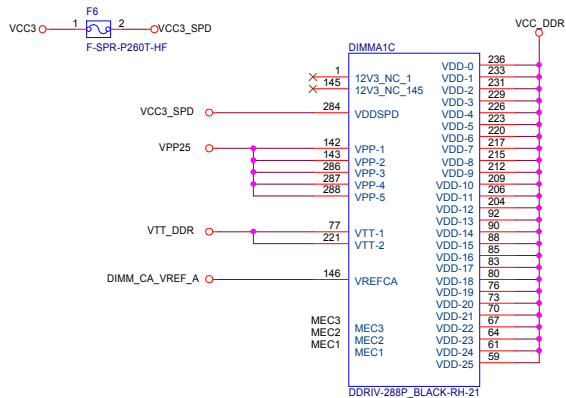


GND

AM4
PART 9 OF 9



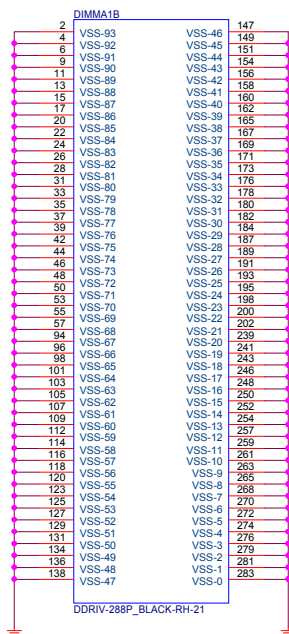
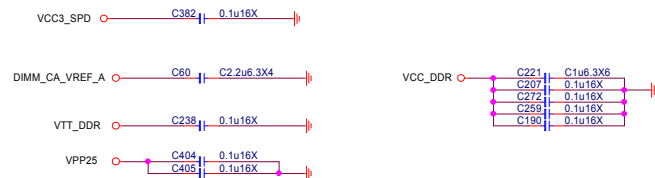
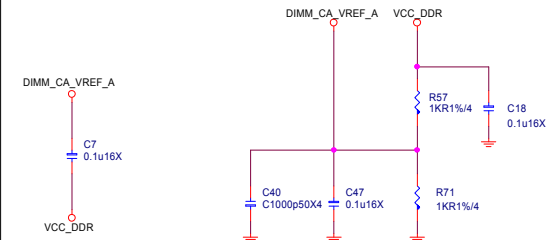


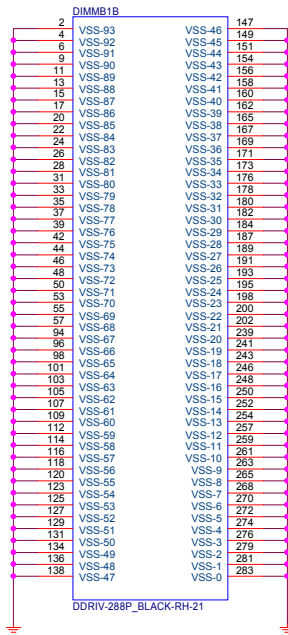
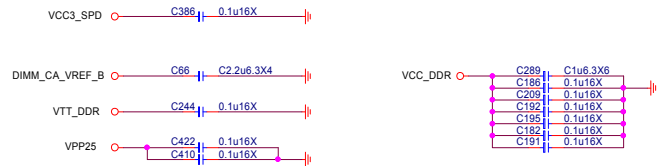
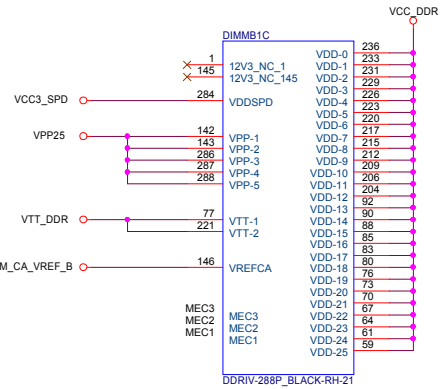


DIMM SLOT PN BY SPEC

DDR VREF

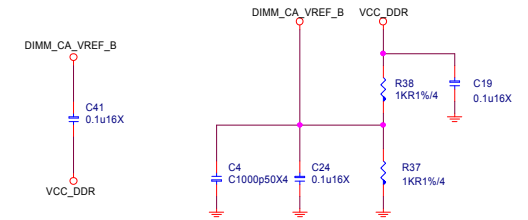
(place resistors close to DIMMs)

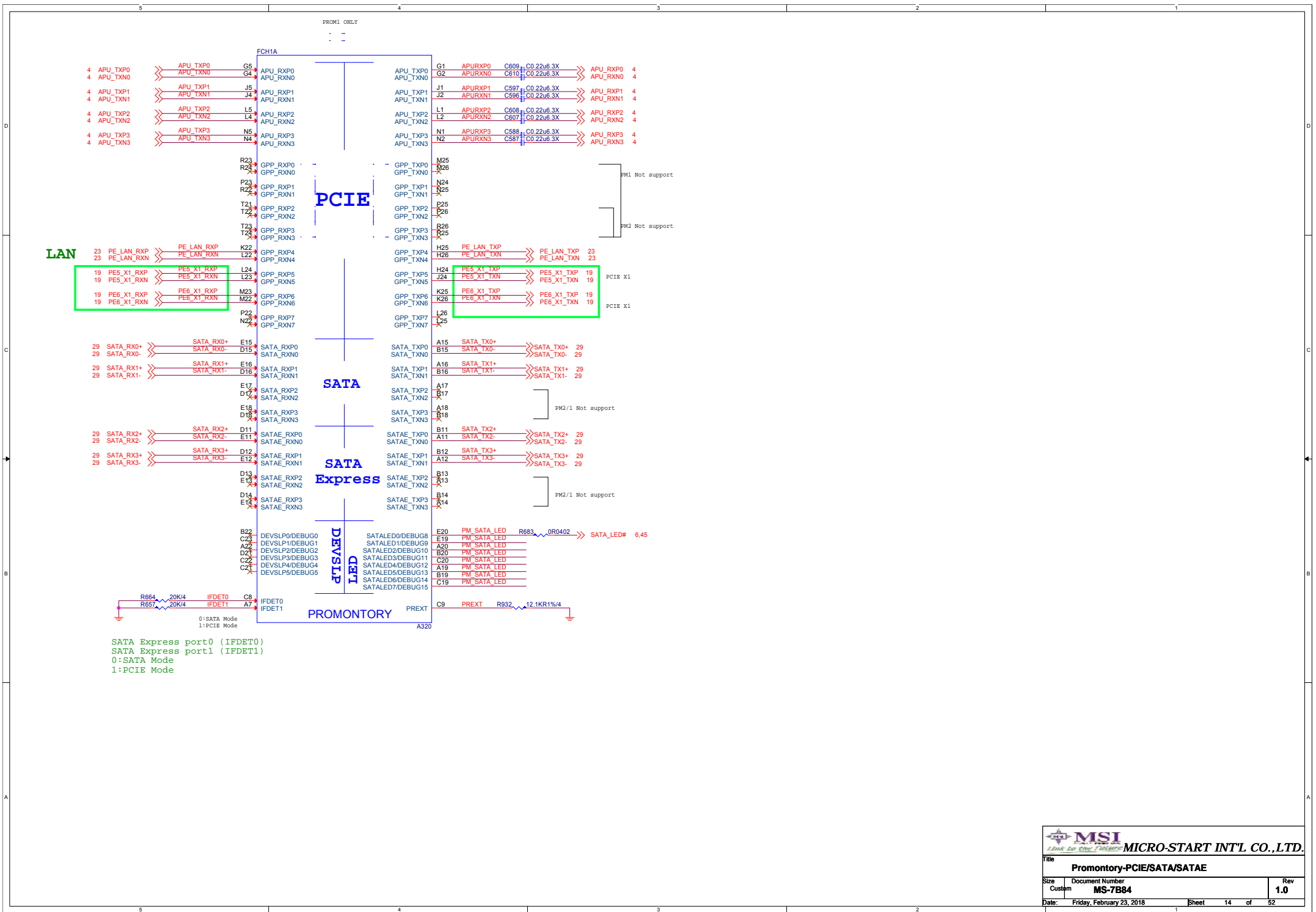




DDR VREF

(place resistors close to DIMMs)





Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXPIN[0]	USB_HSDP[N](5)	USB_OC0N
USB_SSP_TX/RXPIN[1]	USB_HSDP[N](6)	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SSP_TX/RXPIN[0]	USB_HSDP[N](10)	USB_OC2N
USB_SSP_TX/RXPIN[1]	USB_HSDP[N](11)	USB_OC3N
USB_SSP_TX/RXPIN[2]	USB_HSDP[N](6)	USB_OC4N
USB_SSP_TX/RXPIN[3]	USB_HSDP[N](7)	USB_OC5N
USB_SSP_TX/RXPIN[4]	USB_HSDP[N](8)	USB_OC6N
USB_SSP_TX/RXPIN[5]	USB_HSDP[N](9)	USB_OC7N
	USB_HSDP[N](1)	USB_OC7N
	USB_HSDP[N](2)	USB_OC7N
	USB_HSDP[N](3)	USB_OC7N
	USB_HSDP[N](4)	USB_OC7N
	USB_HSDP[N](12)	USB_OC7N
	USB_HSDP[N](13)	USB_OC7N

Appendix C Port Mapping for Different Bus Models

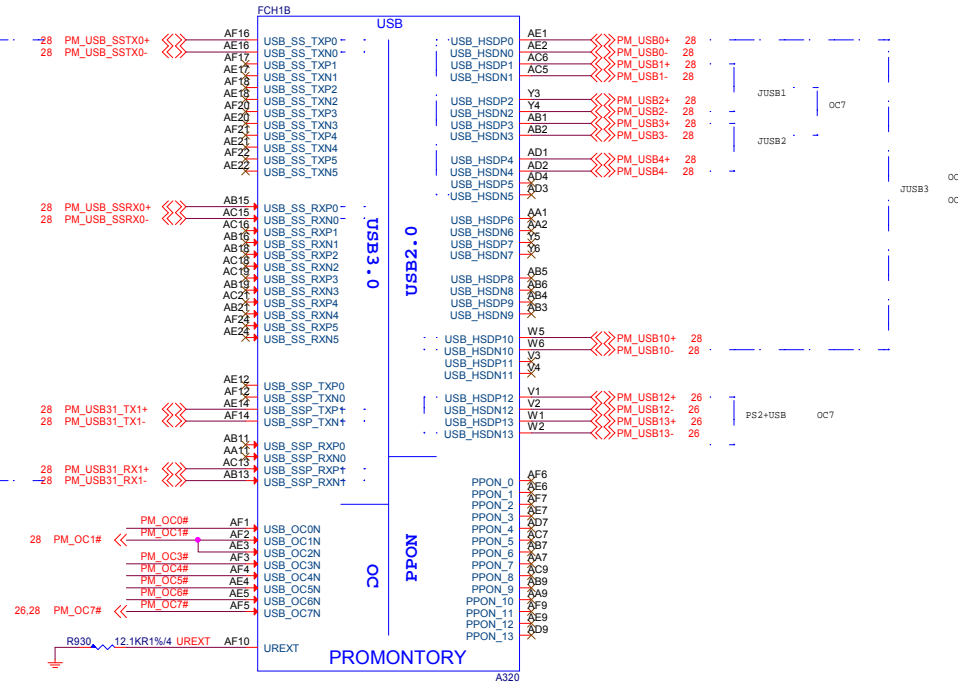
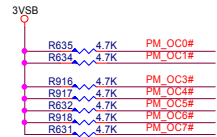
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM14	USB_SSP Port0-1	USB_SS Port0-1	USB_HSD Port0-13	USB_SSP Port0
PROM12	USB_SSP Port0-1	USB_SS Port0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM11	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0

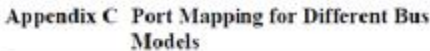
BUS Model	SATA J.0	SATA Express	PCI Express® Gen1 GPP	PCI Express® CLK
PROM14	SATA port0-3	SATAE port0-3	GPP lane0-7	CLK0-7
PROM12	SATA port0-1	SATAE port0-1	GPP lane0-3 GPP lane4-7	CLK0-1 CLK4-7
PROM11	SATA port0-1	SATAE port0-1	GPP lane0-7	CLK4-7

CLK2,3不能
CLK1-3不能

Not supported USB3.0 on PROM2

Not supported USB3.0 on PROM2





B/S Model	USB			
	3.1 Gen2 20 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM14	USB_SSP Port0-1	USB_SS Pair 0-3	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Pair 0-3	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port0	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0

BSV Model	SATA 5.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
FROM4	SATA port0-3	SATAE port0-3	QPP lane4-7	CLK0-3
FROM2	SATA port0-1	SATAE port0-1	QPP lane0-1 QPP lane4-7	CLK0-1 CLK4-7
FROM1	SATA port0-1	SATAE port0-1	QPP lane4-7	CLK4-7

CLK2.3不能用
CLK1-3不能用

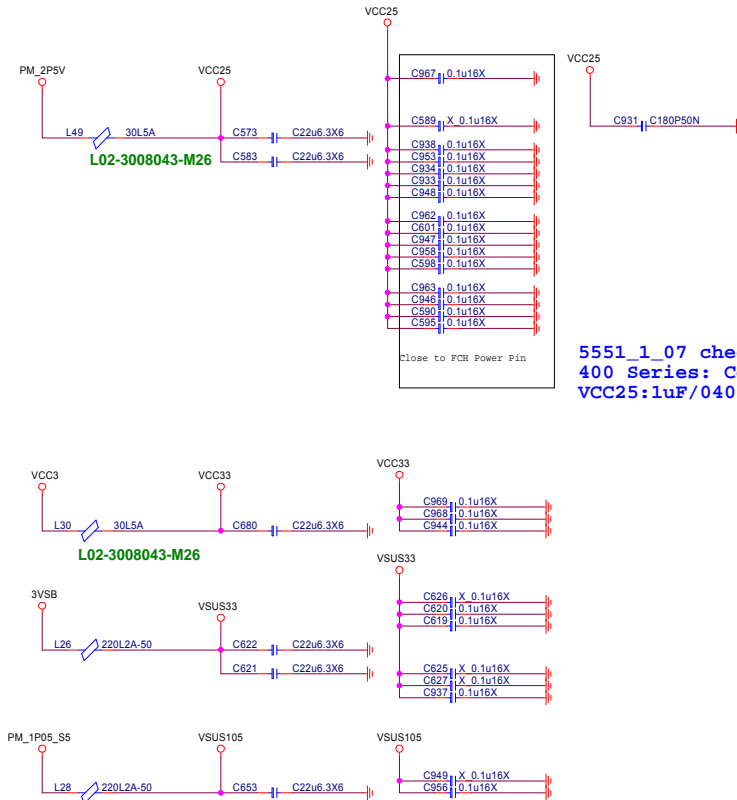
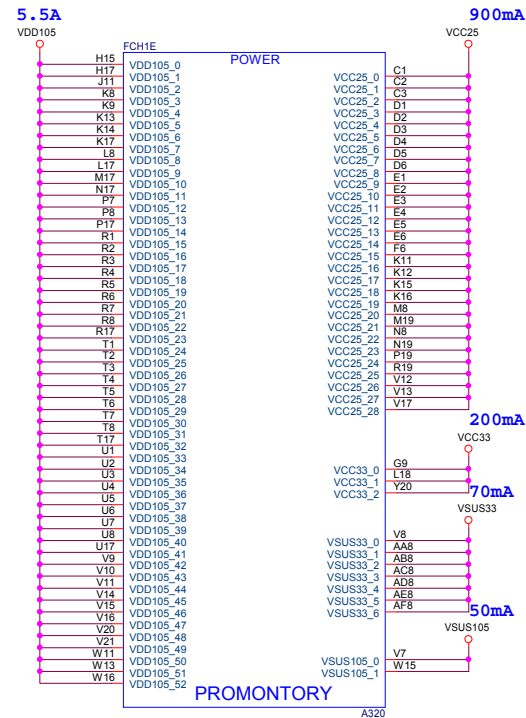
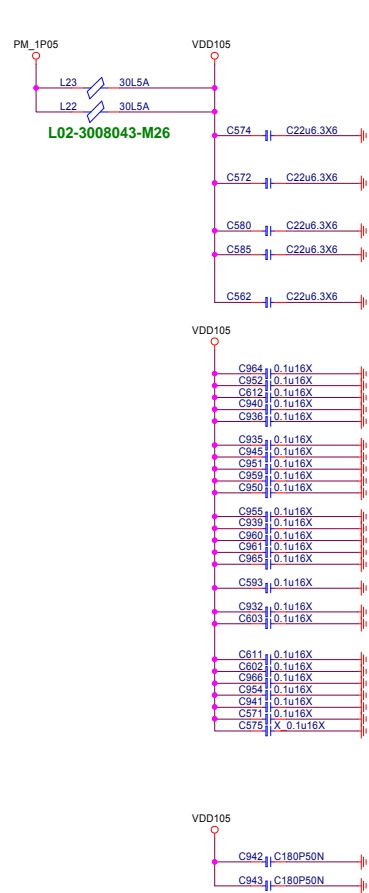
BOM OPTION



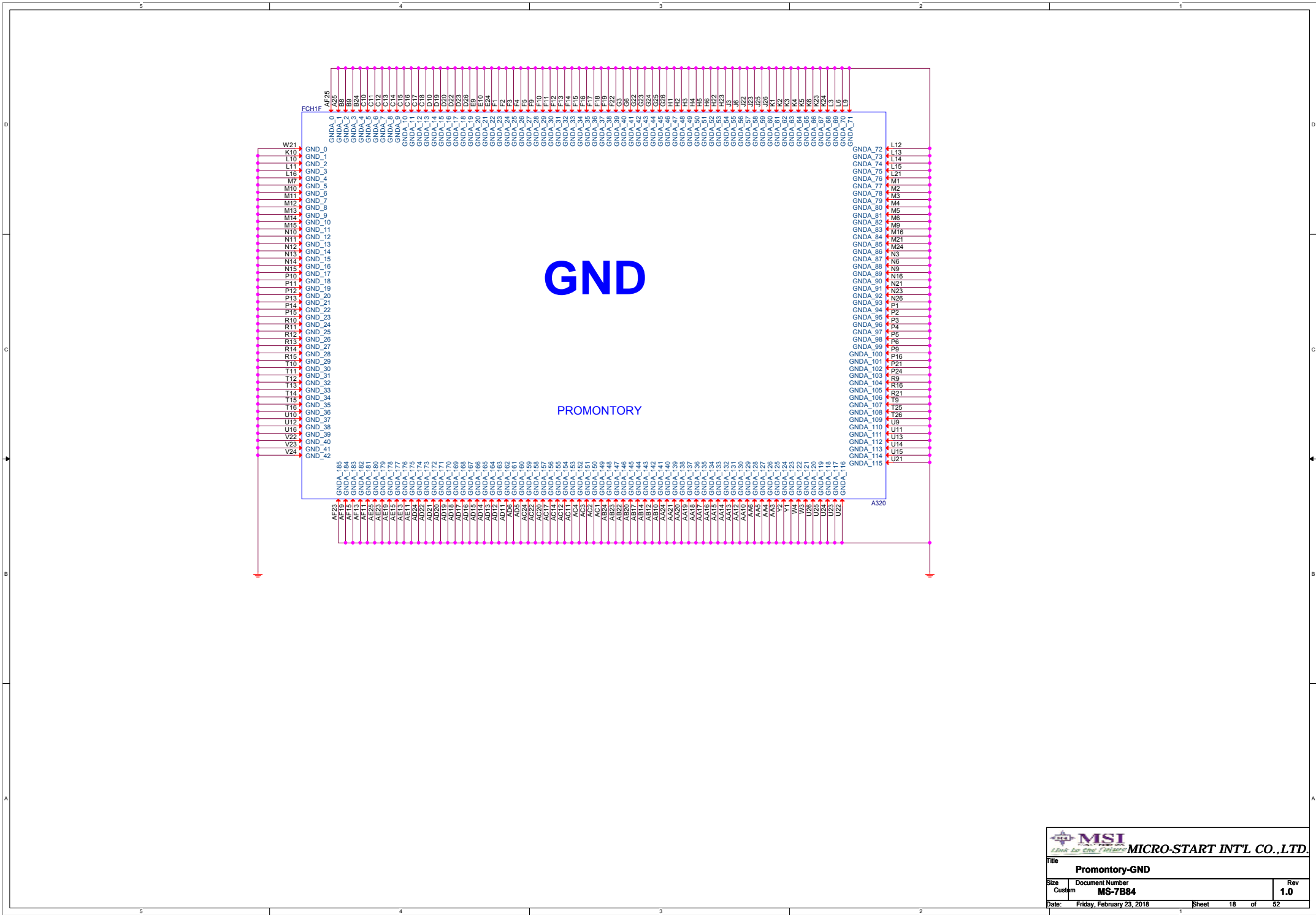
	FULL	
GPIO2	0	
GPIO3	0	
GPIO4	0	

 **MSI**
Look to the Future MICRO-START INT'L CO., LTD.

Title				
Promontory-CLK/ACPI/GPIO				
Size	Document Number			Rev
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5551_1_07 check list
400 Series: Ceramic capacitors.
VCC25:1uF/0402



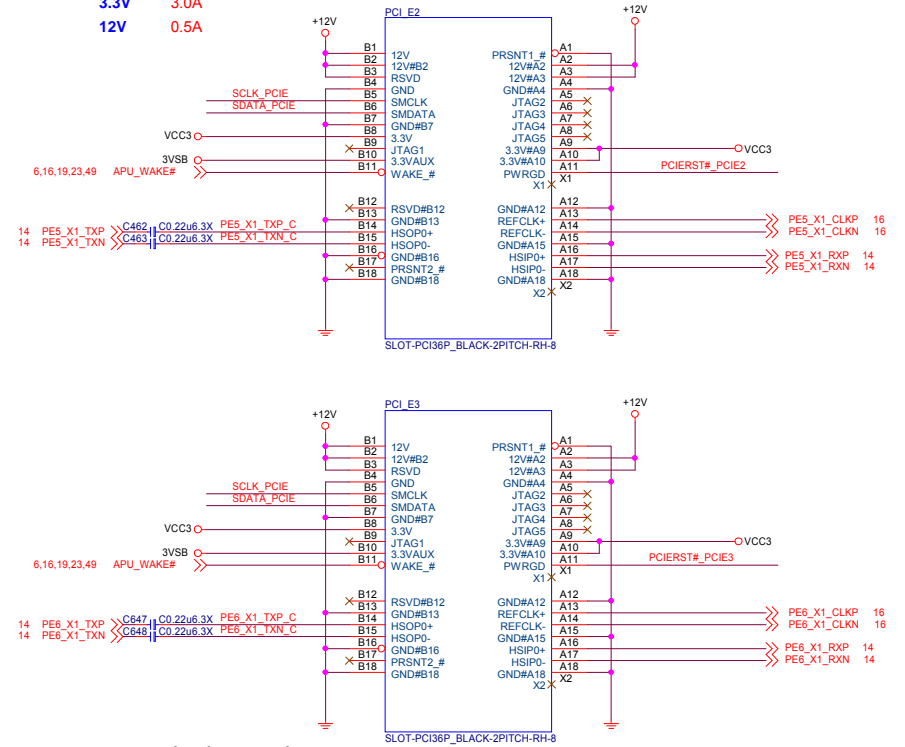
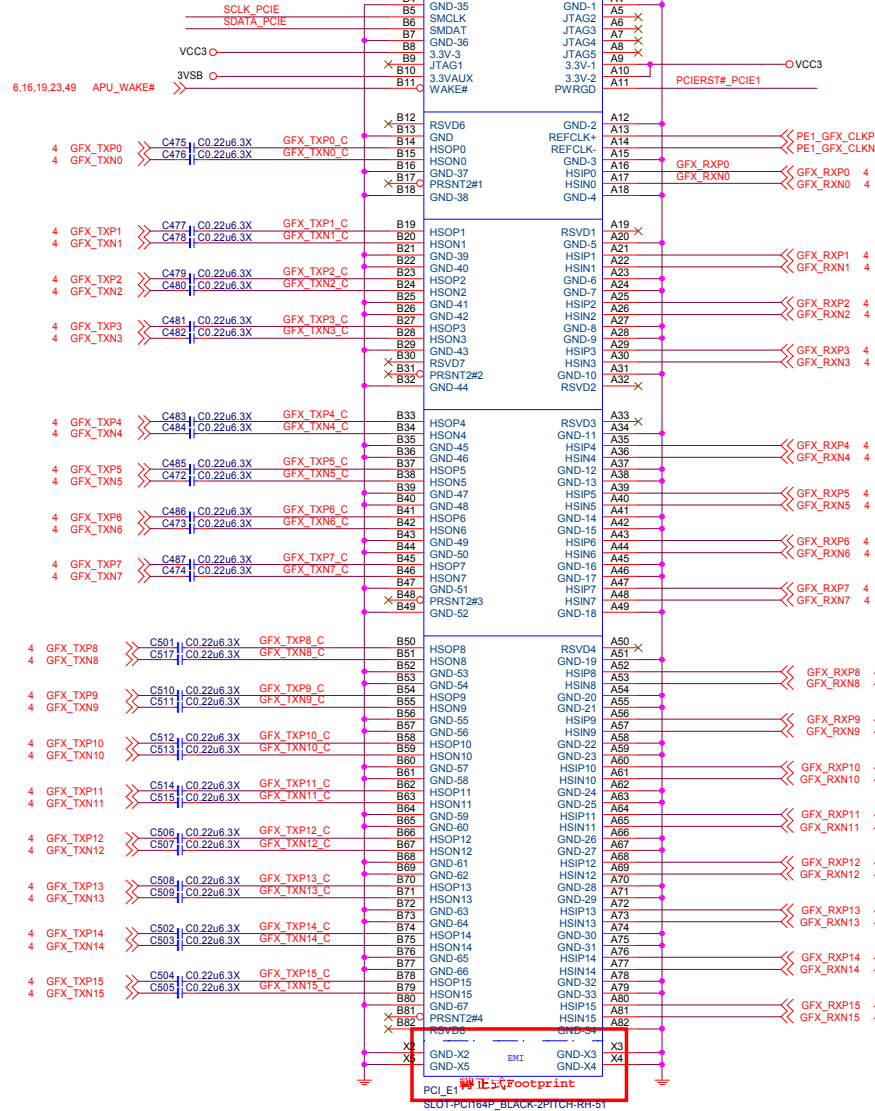
20170413 PCIe Slot change to N11-1641491-L06

PCI EXPRESS x16 Slot

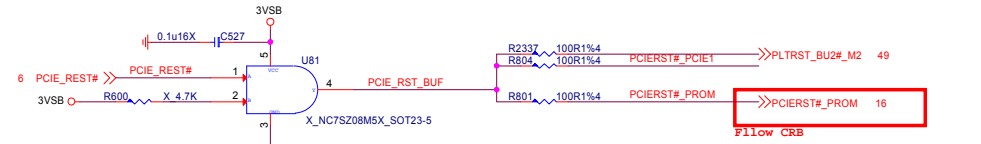
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A

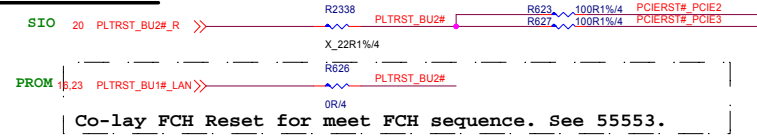
Trace width > 200 mils



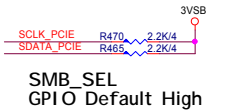
within 500mil



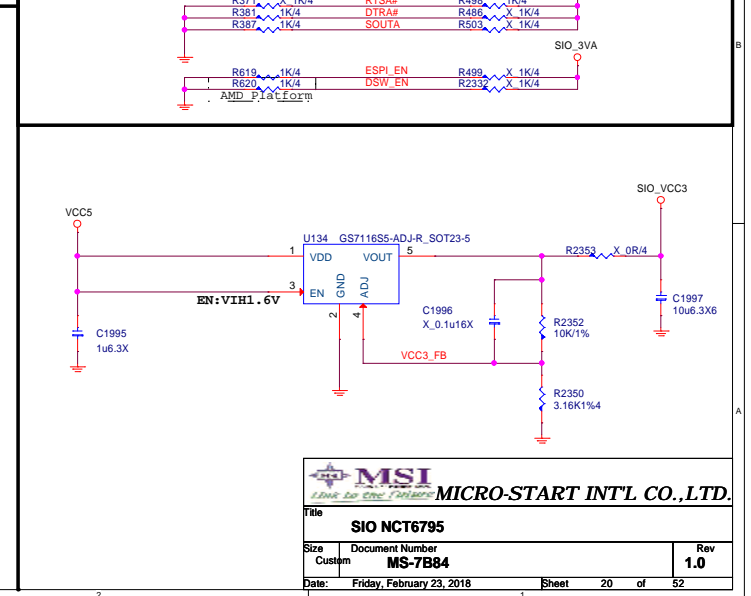
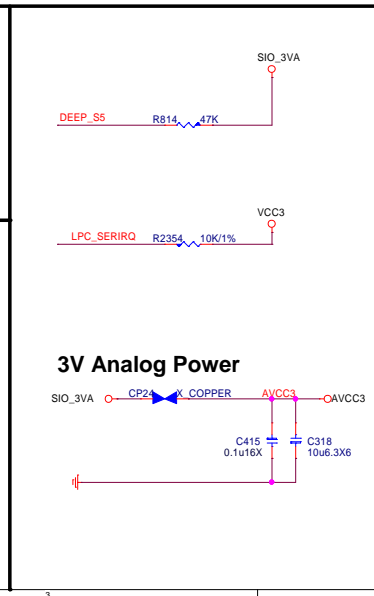
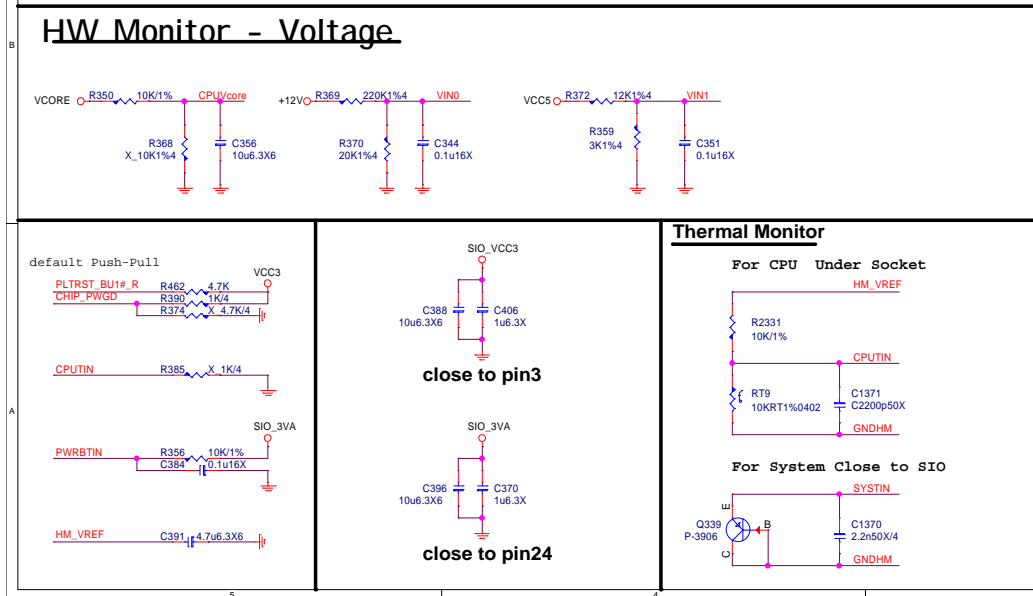
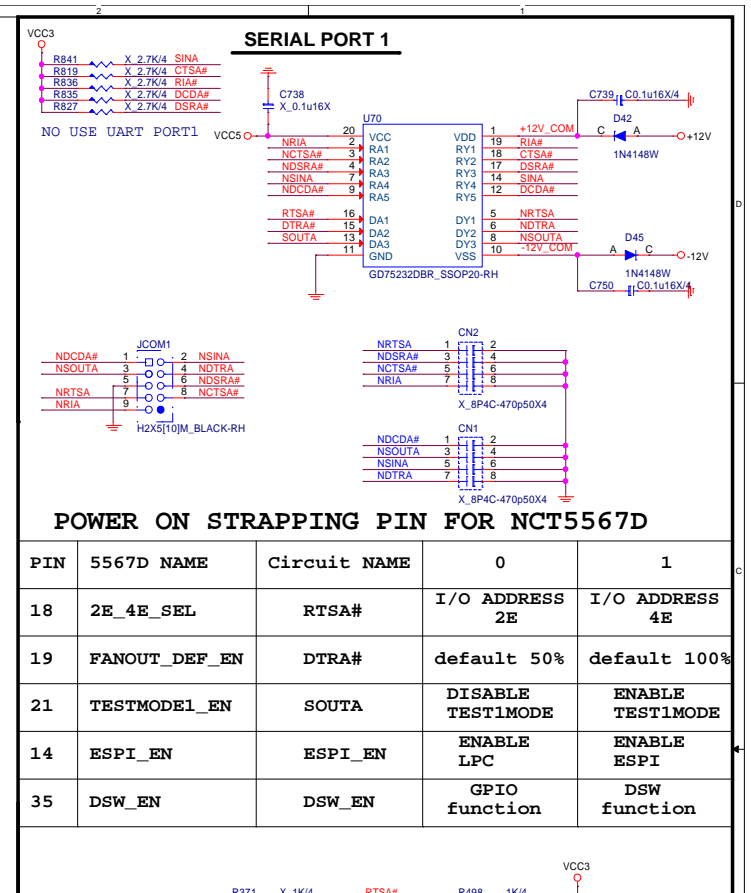
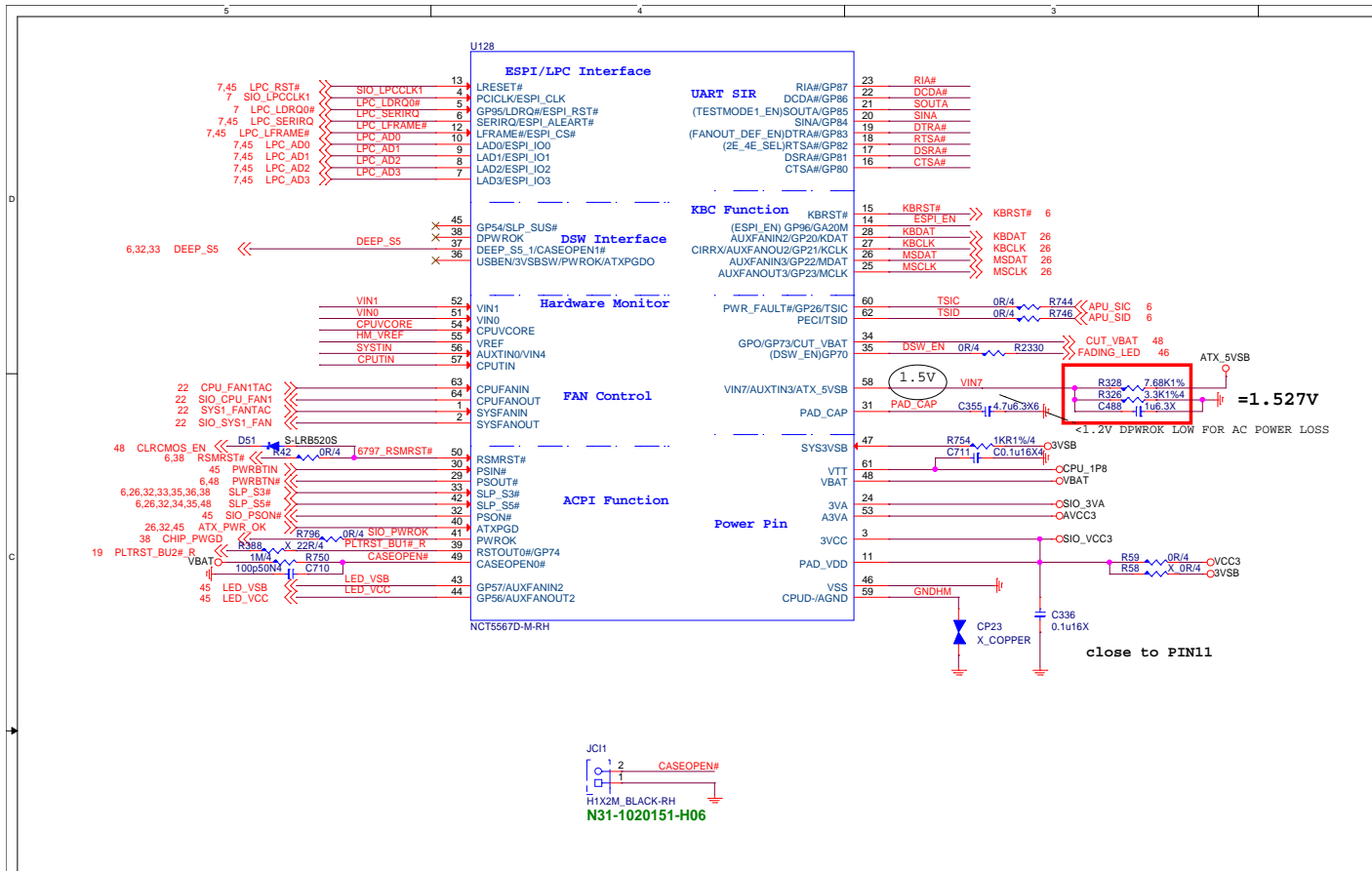
PROM RESET



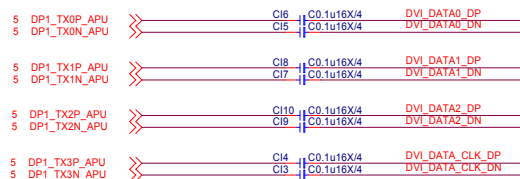
SMBus separate circuit



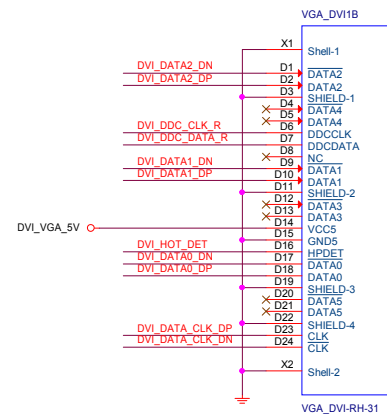
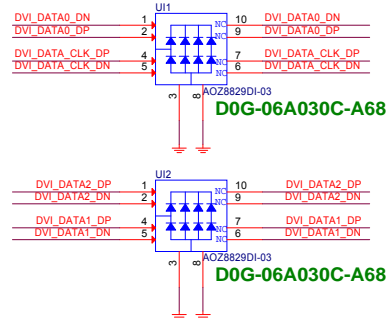
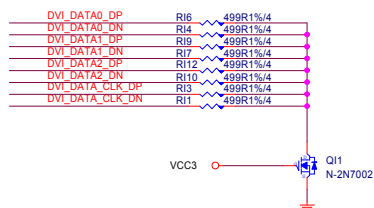
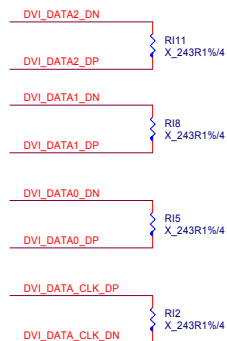
<p>MSI MICRO-START INTL CO.,LTD.</p>		
File	PCI E X16(X1*2) SLOT	
Size	Document Number	Rev
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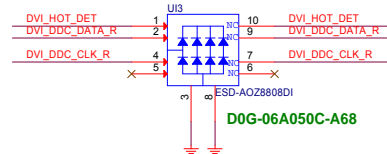
DVI CONNECTOR



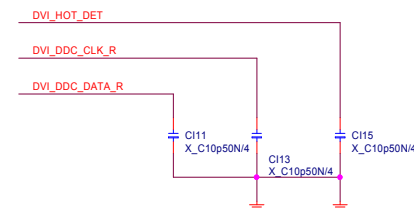
For EMI



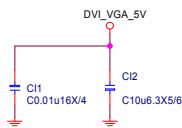
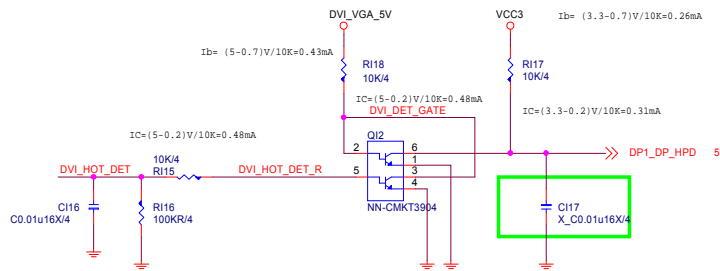
注意:耐壓5V零件



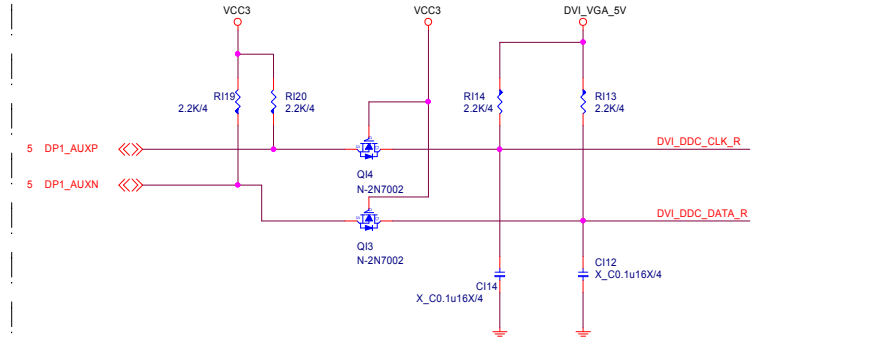
For EMI



HPD



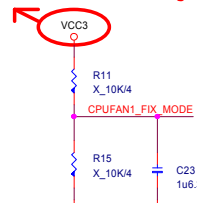
LEVEL SHIFT using I2C Repeater



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

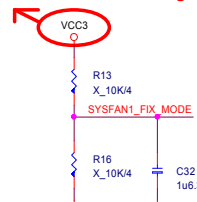
2.GPIO可以由BIOS切换 PWM/DC MODE

Avoid NCT3947S MODE PIN Leakage

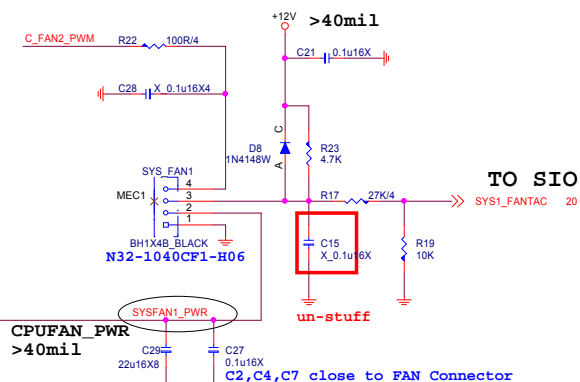
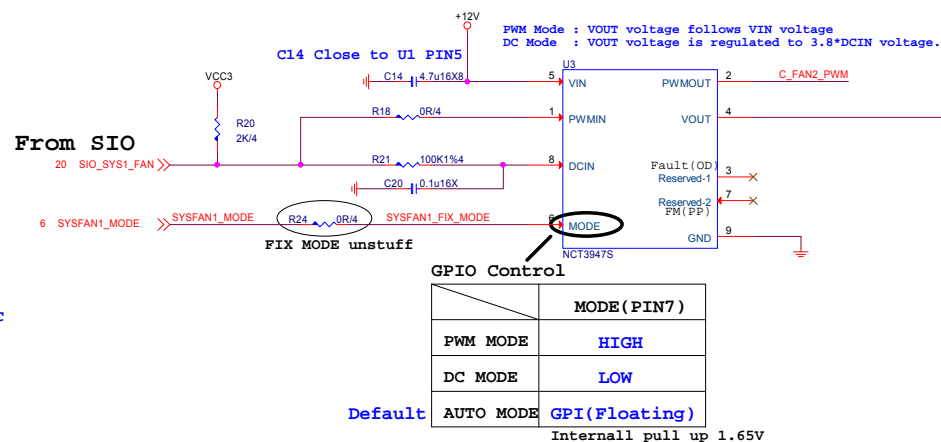
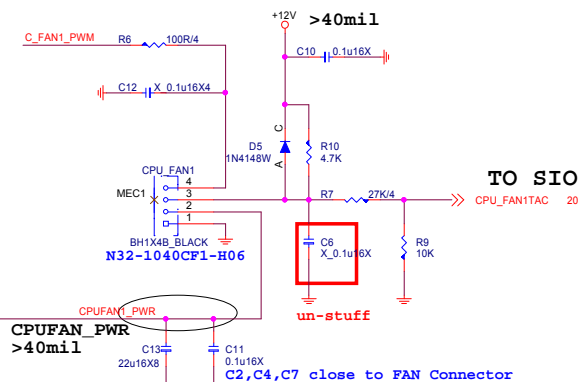
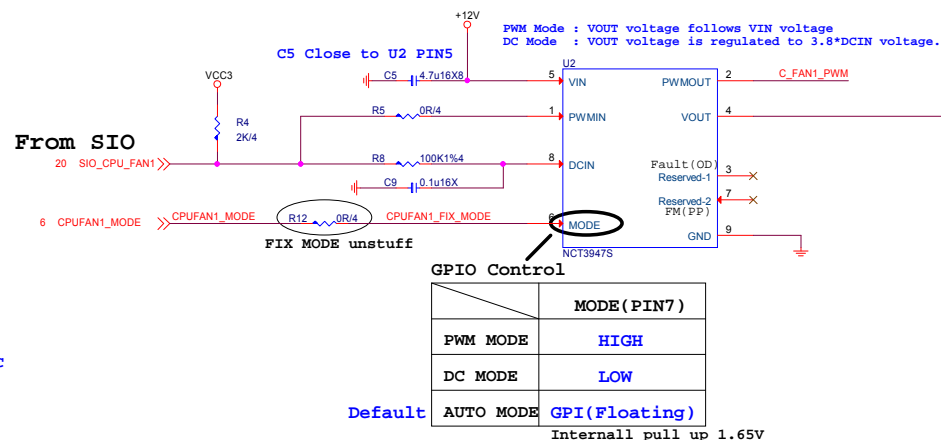


Resever For FIX DC or PWM MODE USE By PM SPEC

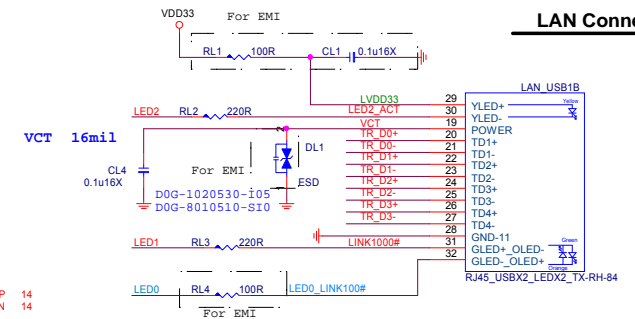
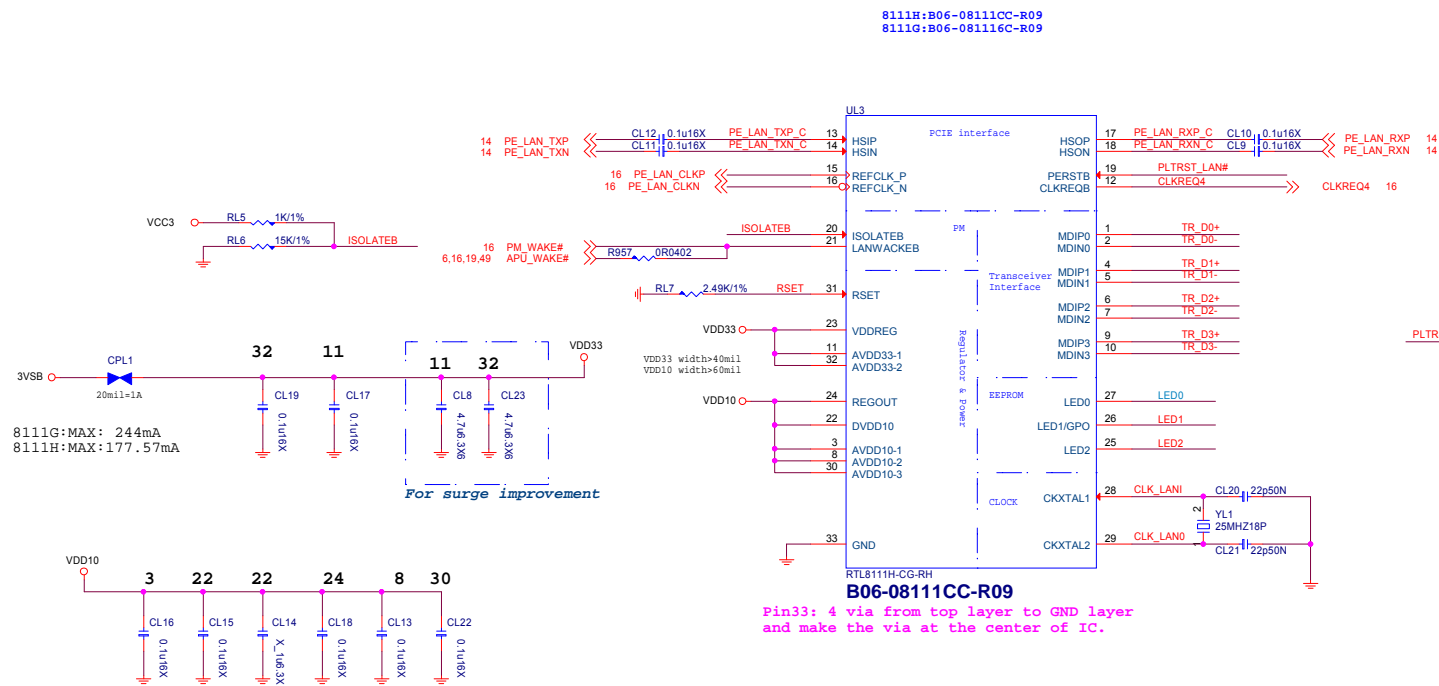
Avoid NCT3947S MODE PIN Leakage



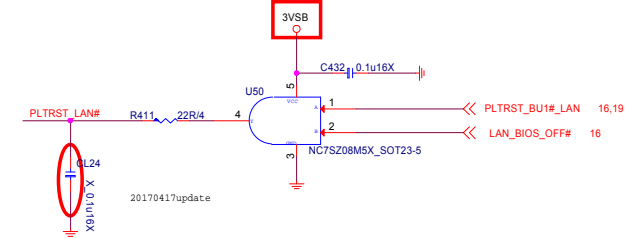
Resever For FIX DC or PWM MODE USE By PM SPEC



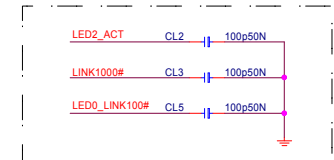
RTL8111G/RTL8111H Giga LAN



20170413 VCC3 change to 3VSB



For EMI 2015.06.22



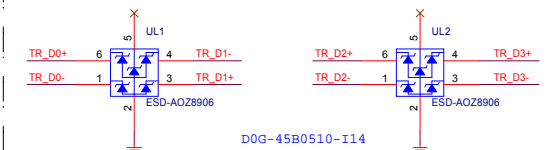
8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

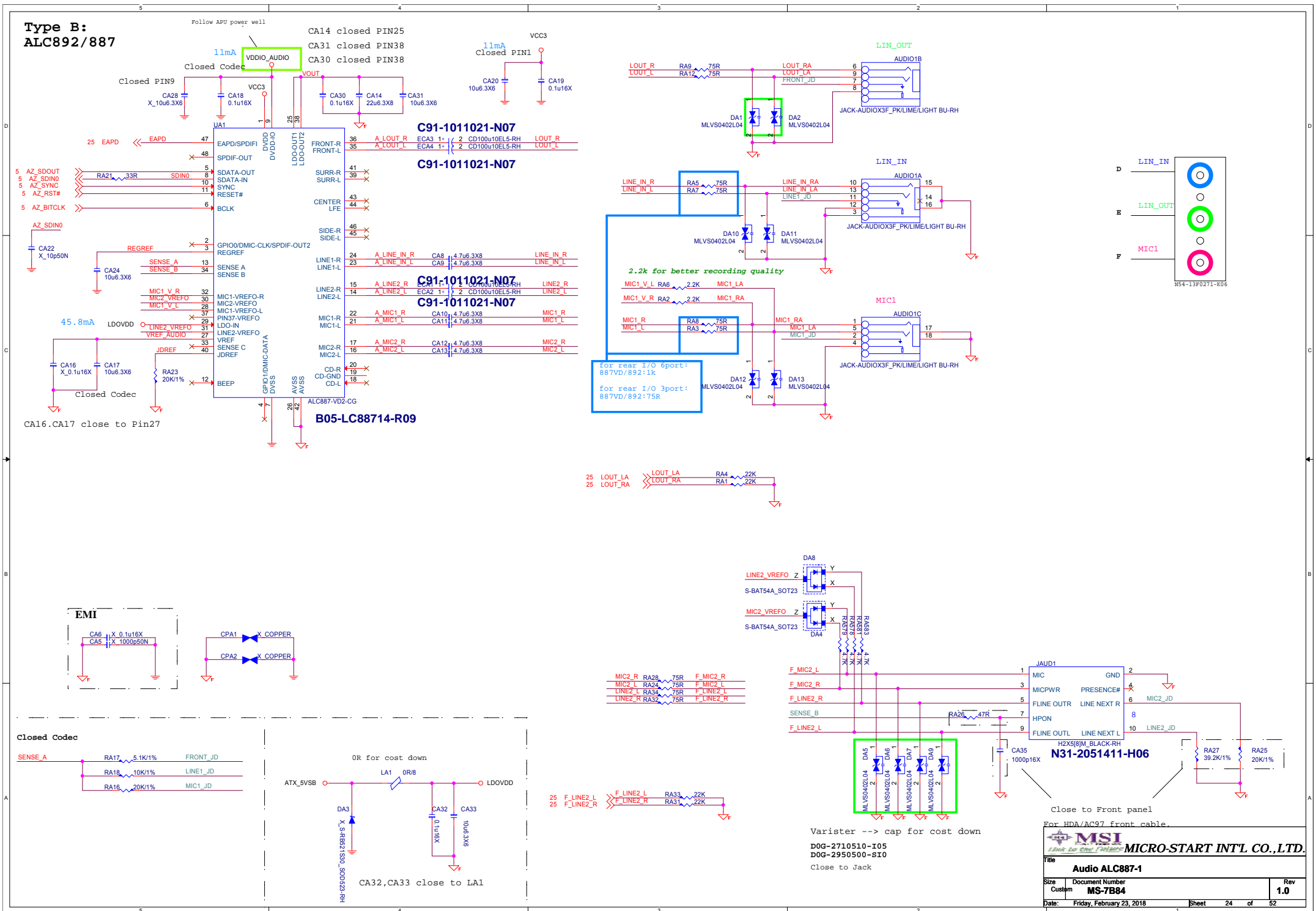
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

ESD Protect
UL2&UL3 close to connector

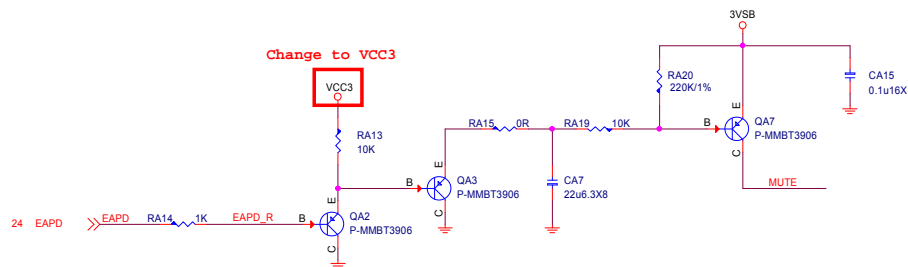


Type B:
ALC892/887



Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

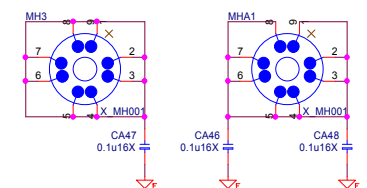


Digital

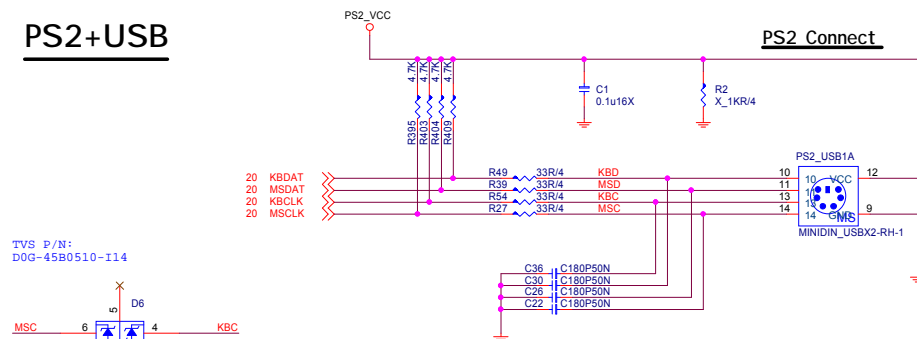
Analog



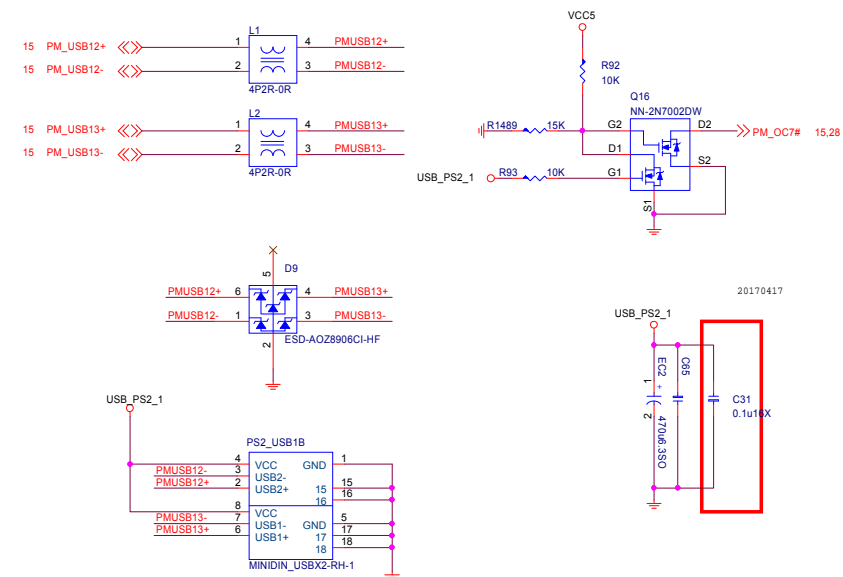
使用漏光LED



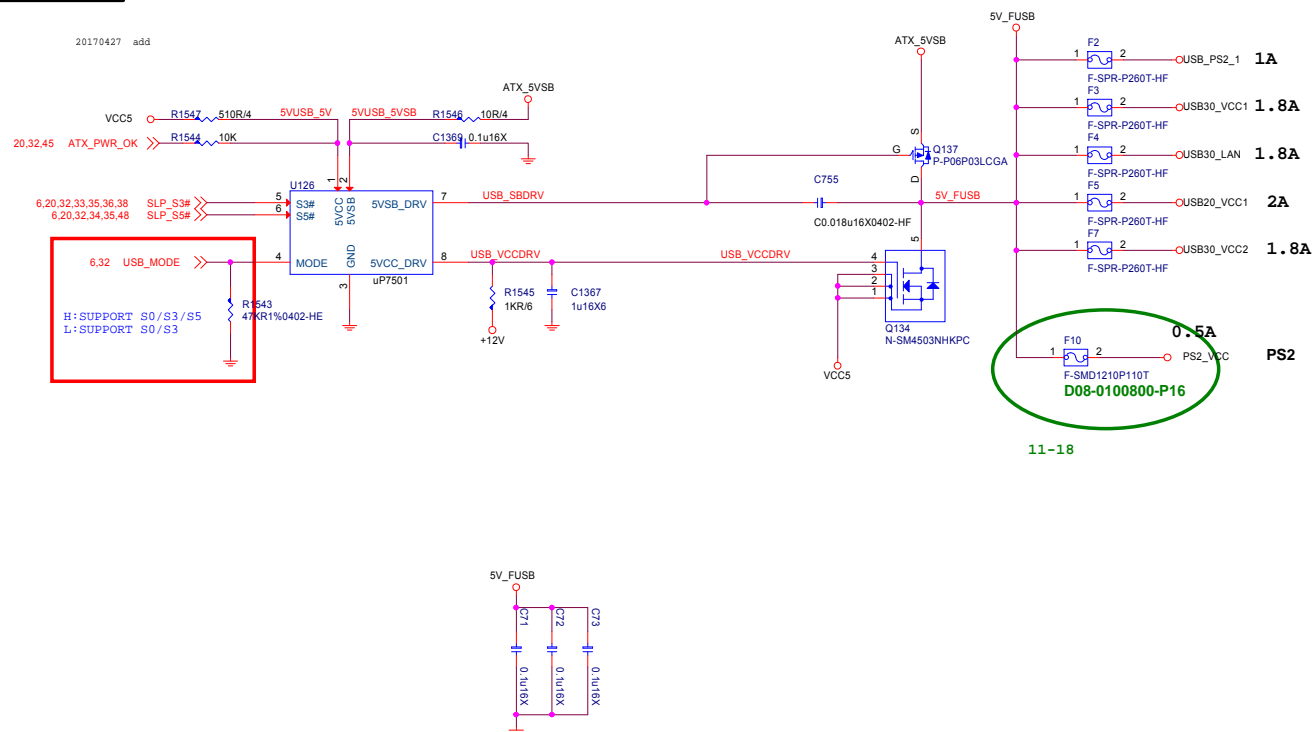
TVS P/N:
D0G-45B0510-I14



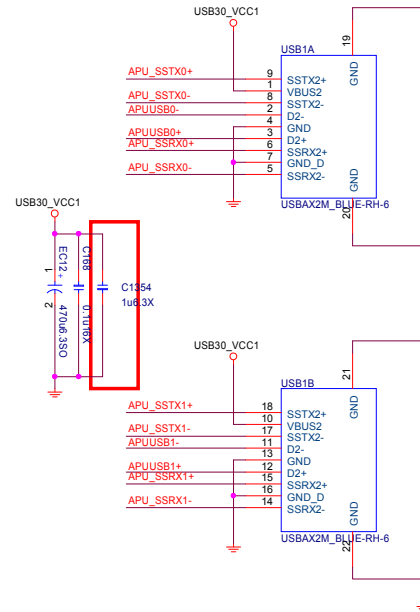
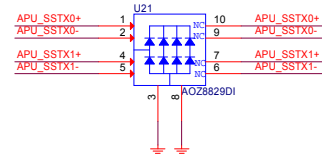
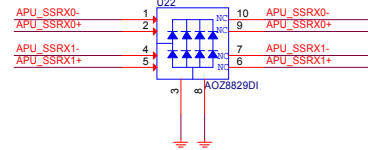
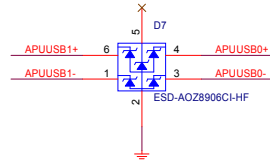
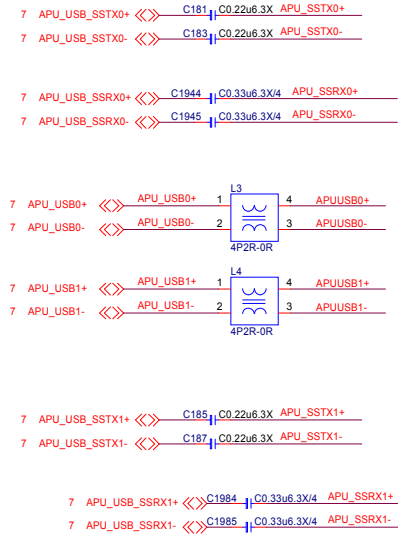
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



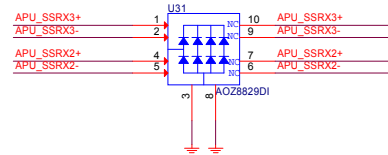
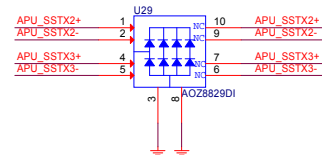
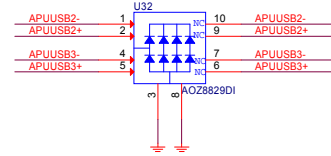
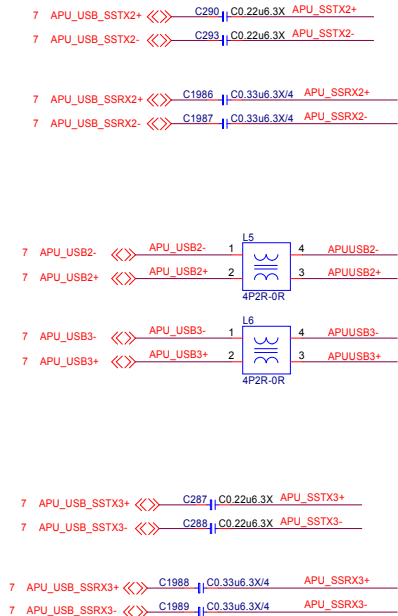
```
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
```



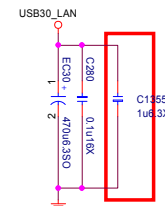
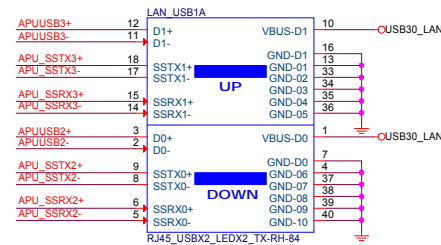
USB 3.0



USB3.1 GEN1

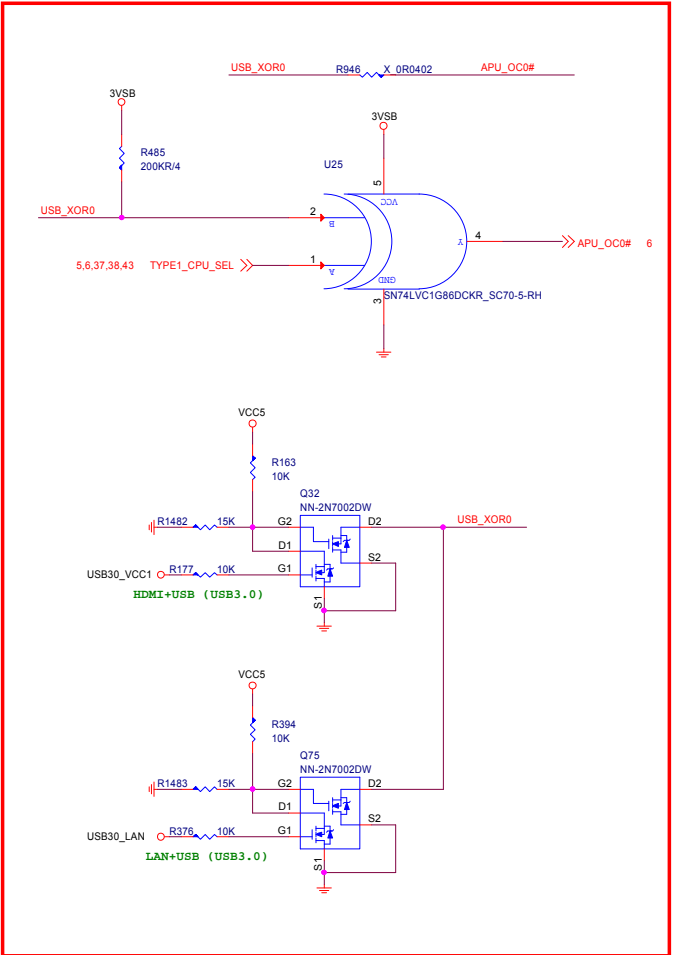


LAN+USB



APU_USB_OC

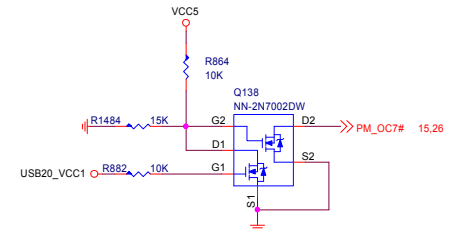
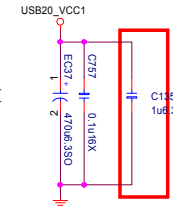
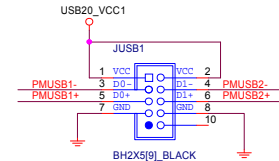
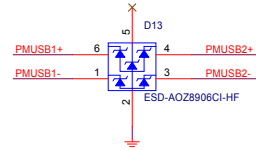
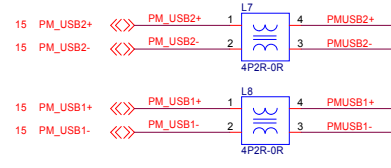
Modify USB_OC# circuit



	CORETYPE(A)	USB FWR(B)	APU USB OC(Y)
TR	0	0	0
Act.Low	0	1	1
SR	1	0	1
Act.High	1	1	0

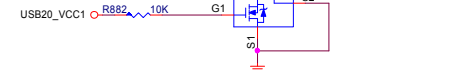
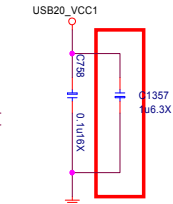
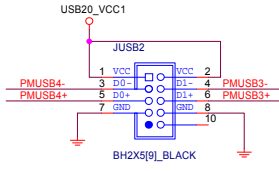
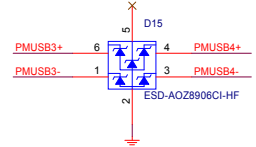
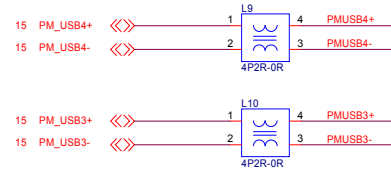
Front USB2.0(JUSB1)

5V@1A

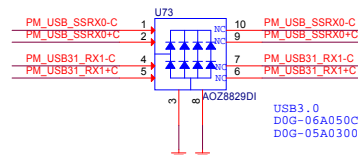
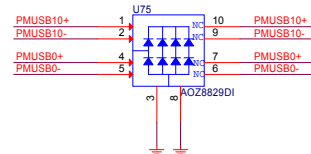
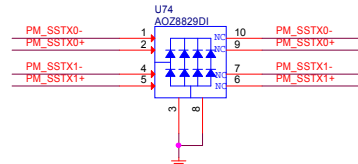
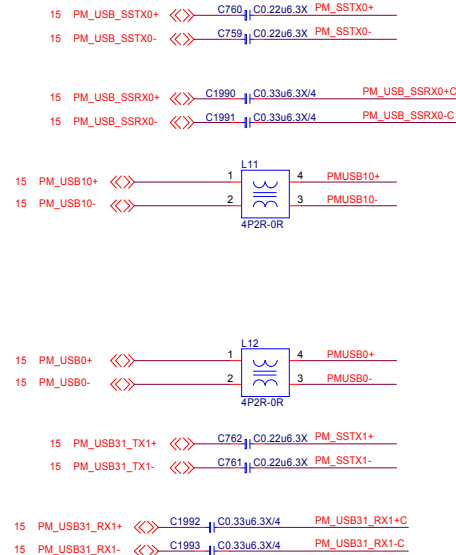


Front USB2.0(JUSB2)

5V@1A

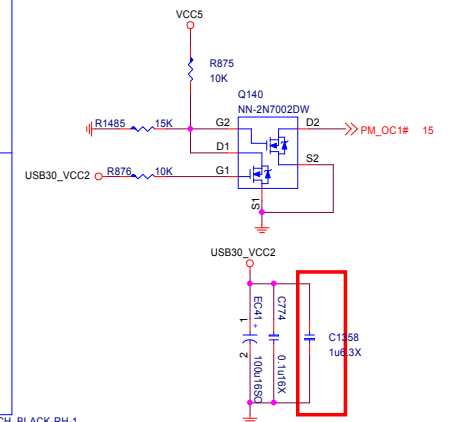
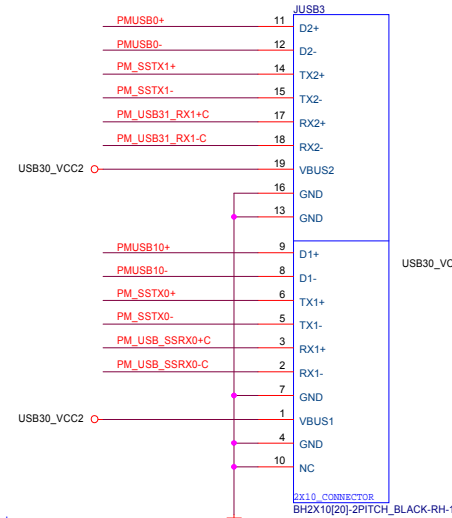


Front USB3.1 GEN1

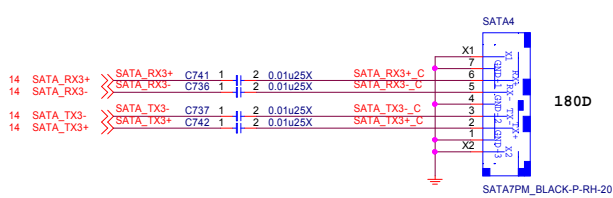
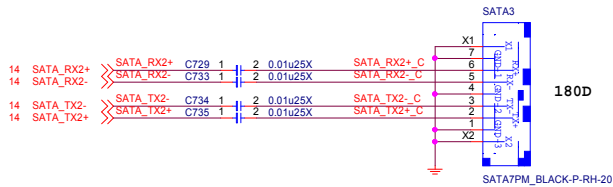
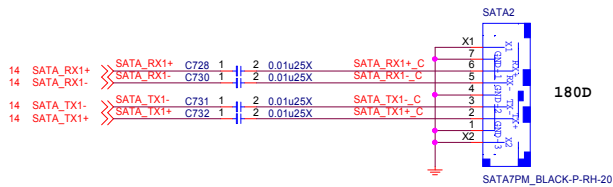
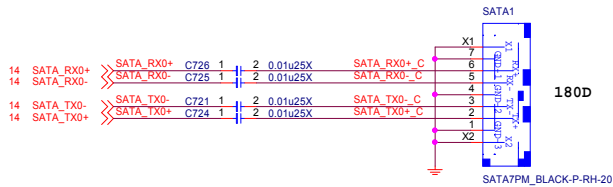


USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

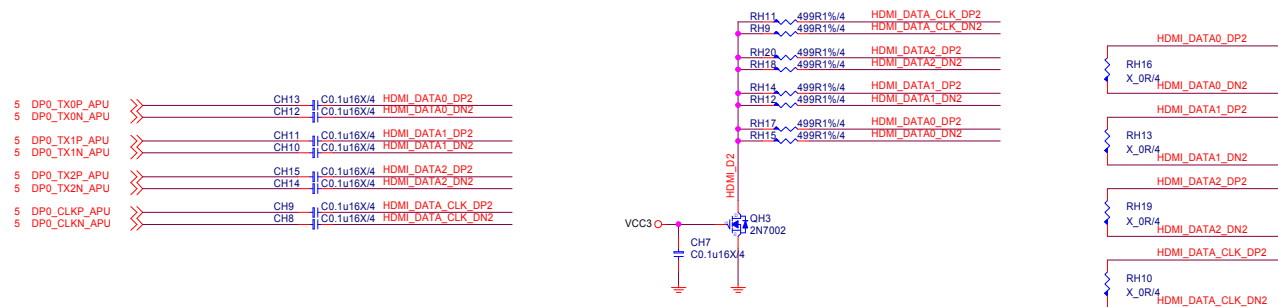
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



SATA Connector



For HDMI 1.4



$I_B = (V_{CC5} - V_{be}) / 10k$
 $(5 - 0.95) / 10k = 0.405mA$
 $I_C = (V_{CC3} - V_{ce}) / 4.7k$
 $(3.3 - 0.2) / 4.7k = 0.659mA$

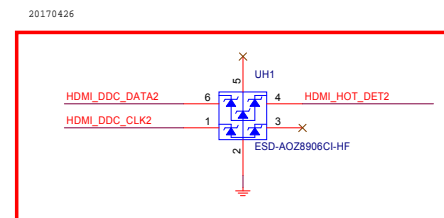
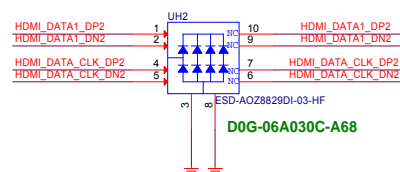
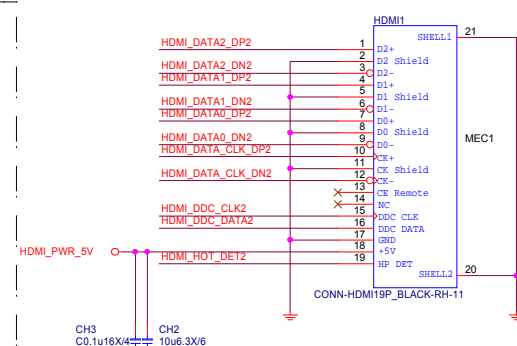
$I_B = (V_{CC5} - V_{be}) / 10k$
 $(5 - 0.95) / 10k = 0.405mA$
 $I_C = (V_{CC5} - V_{ce}) / 10k$
 $(5 - 0.2) / 10k = 0.48mA$

Diagram illustrating the connection for testing the HDMI PWR_5V pin of the D08-3010K09-U47 module.

The circuit shows a +12V supply connected through a resistor (R98, 10K/4) to the GND pin (Q17) of the module. The module is identified as D08-0100800-P16.

The module's FS1 pin (F-SMD1210P110TFT-HF) is connected to the HDMI_PWR_5V pin (2). The HDMI_PWR_5V pin is also connected to a red wire labeled HDMI_PWR_5V.

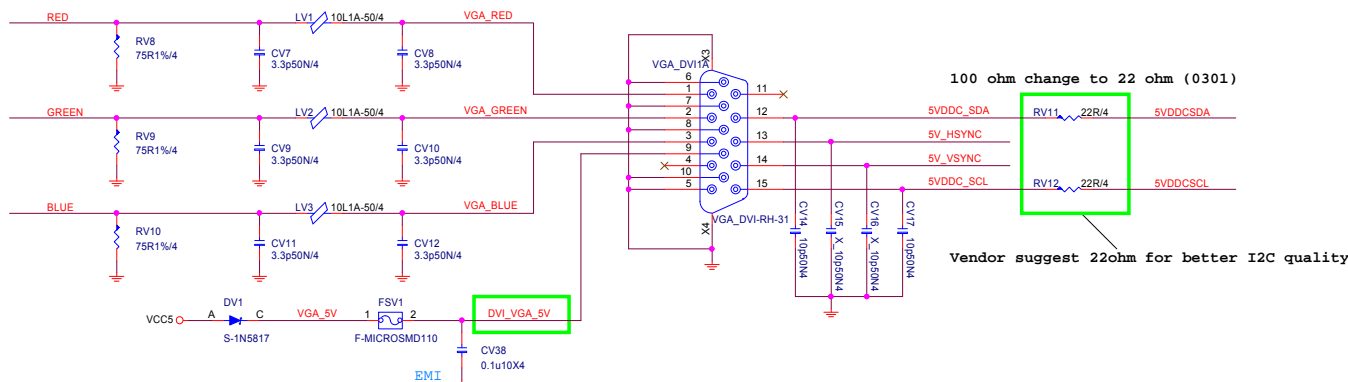
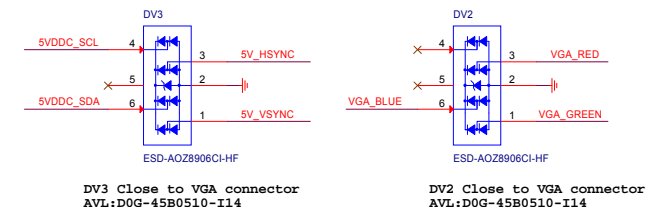
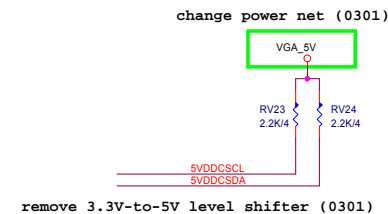
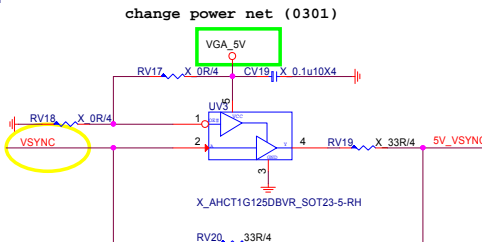
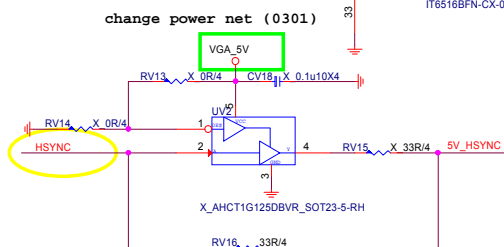
The module is identified as D08-0100800-P16.



If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



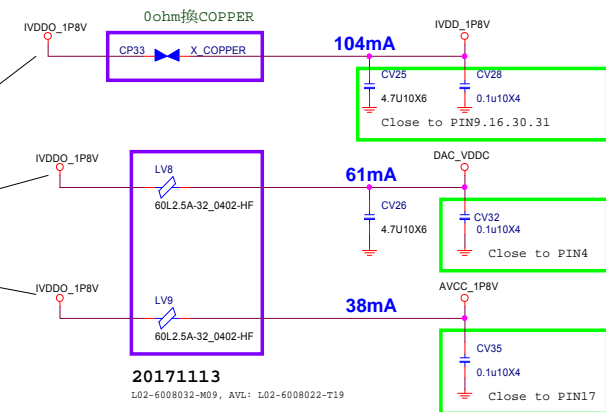
System Status	GPIO	116016b 8 H1D
Legacy Mode (VBIOS) /HOS MODE	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/inplug



100 ohm change to 22 ohm (0301)

Vendor suggest 22ohm for better I2C quality

```
add D-sub function 0225
```

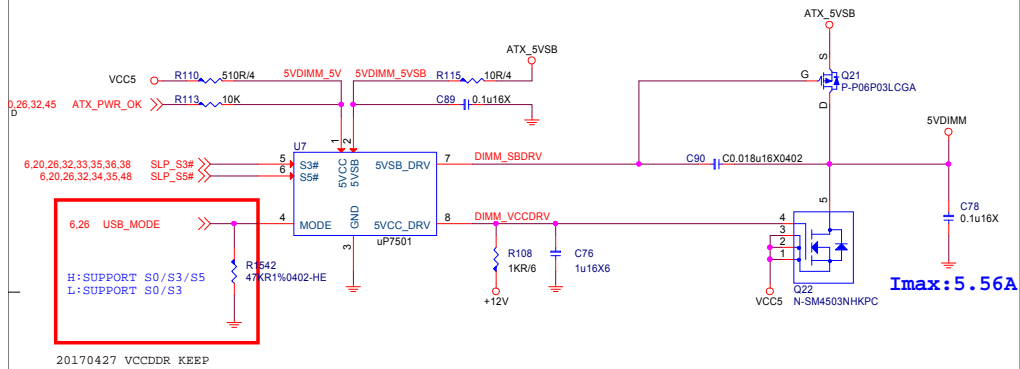


20171113
L02-6008032-M09, AVL: L02-6008022-T19

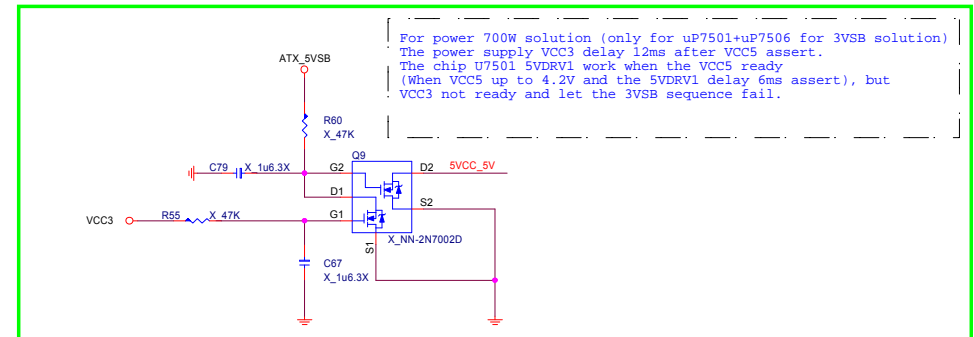
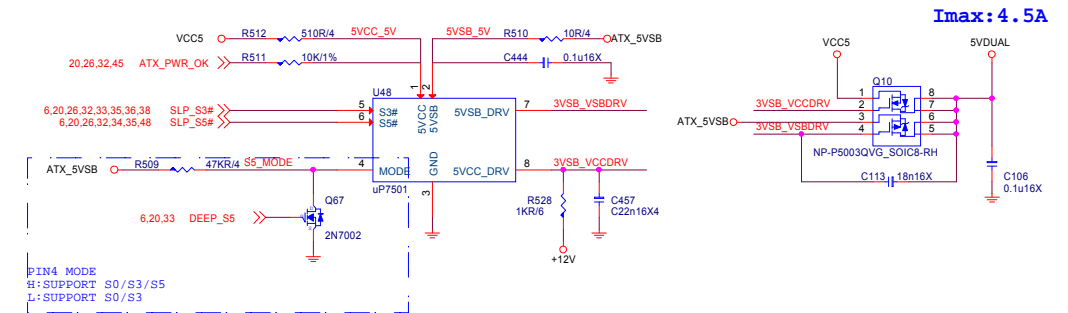
change power net (0301)

```
remove 3.3V-to-5V level shifter (0301)
```

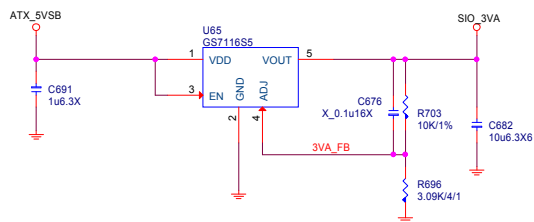
5VDIMM FOR DDR



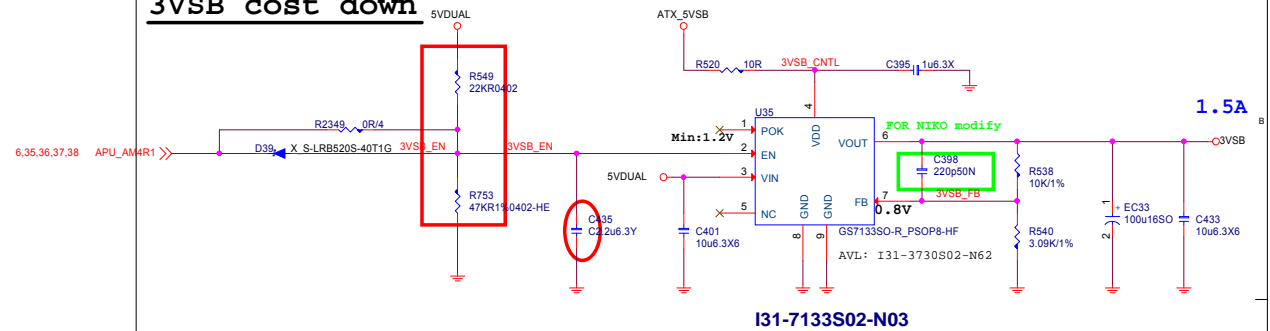
5VDUAL For 3VSB、CPU 1.8V、VDDP



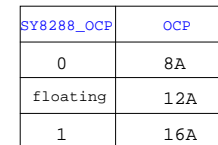
SIO_3VA



3VSB cost down

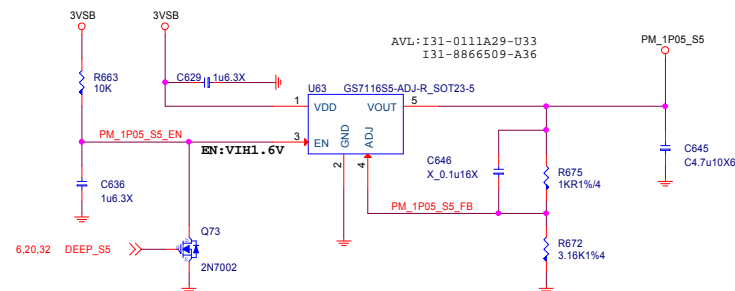


1.05V
S0:5.5A
S5:0.05A

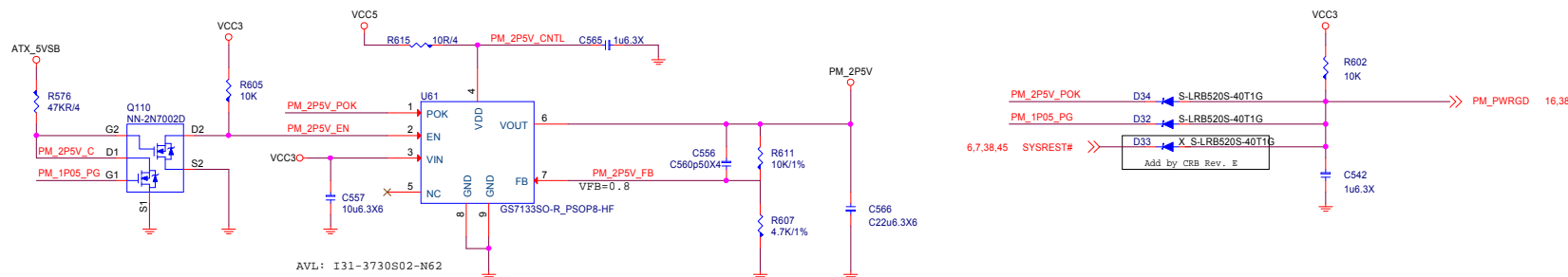


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (1K/1.33K)) \\ &= 1.051V \end{aligned}$$

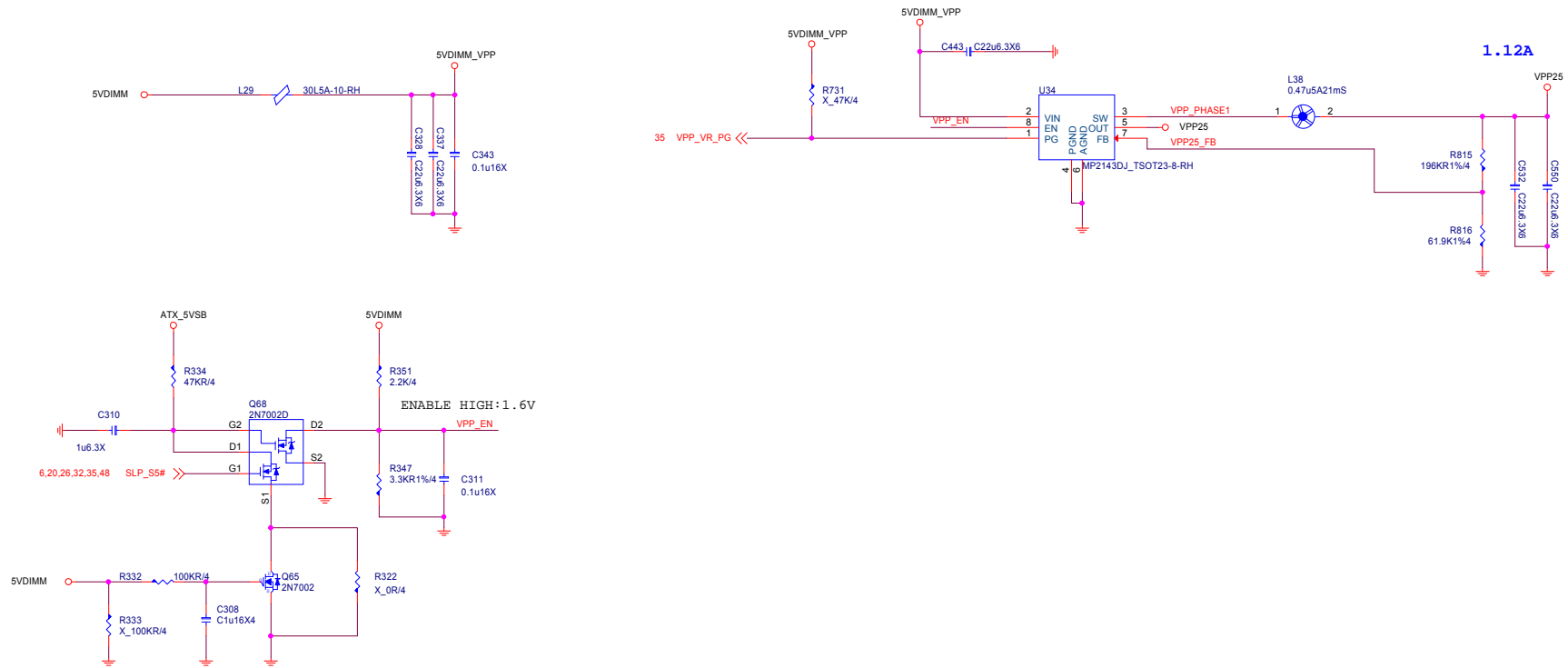
$0.05A$



2.5V; 900mA



2DIMM : 1.12A FOR DDR VPP2.5V

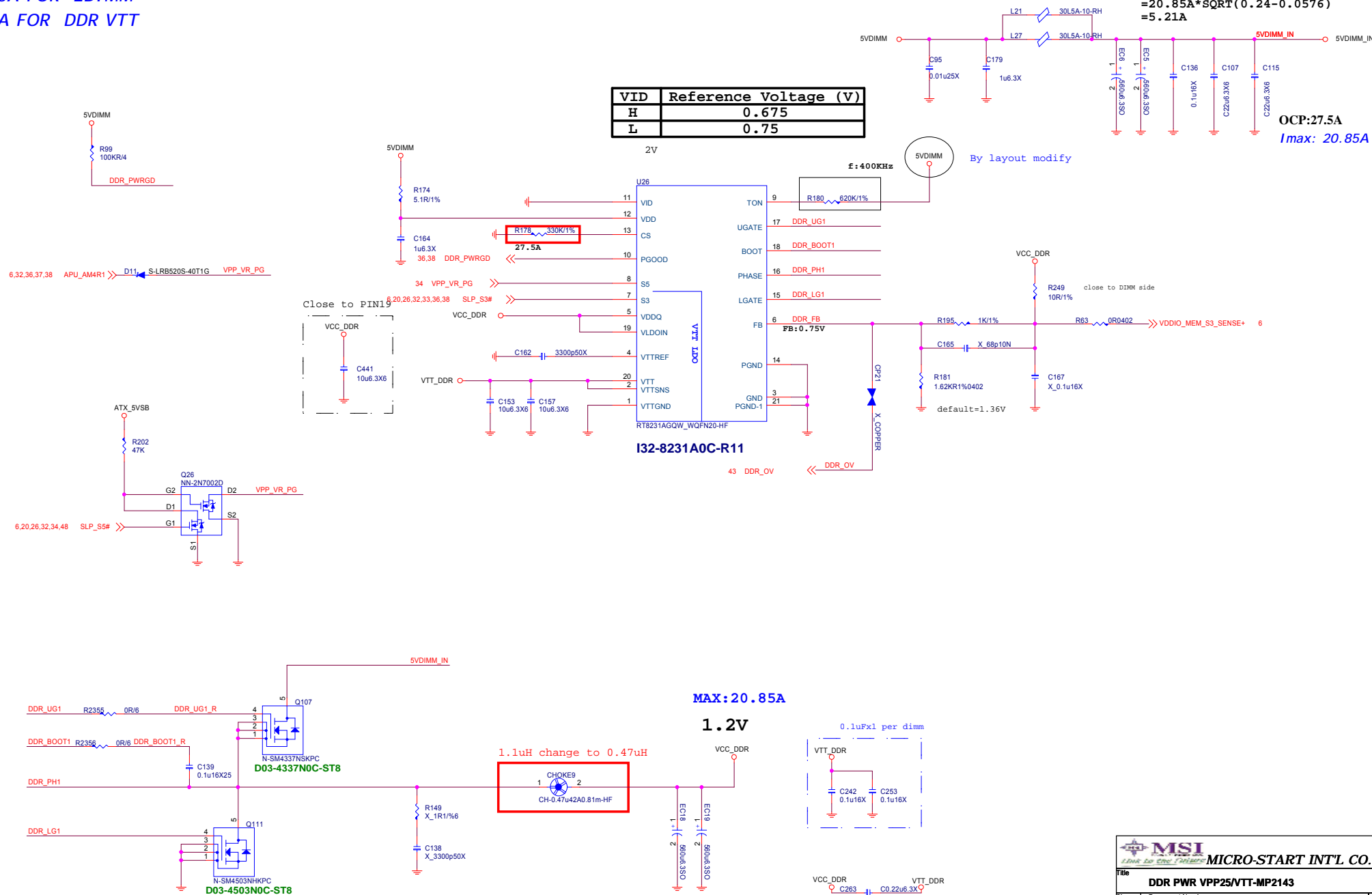


15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

```
Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A
```

VID	Reference Voltage (V)
H	0.675
L	0.75


OCP:27.5A
I_{max}: 20.85A

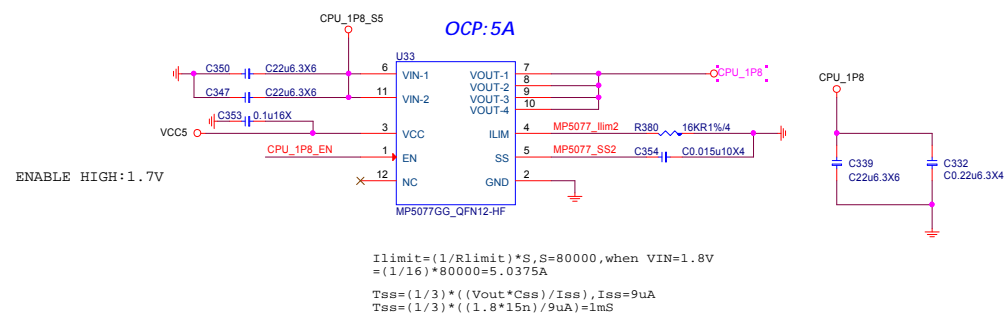
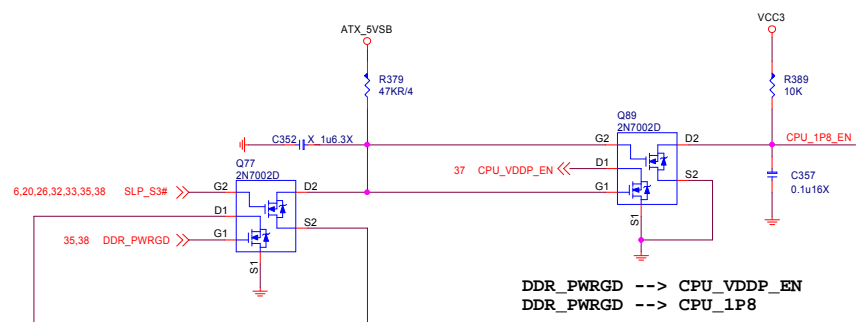
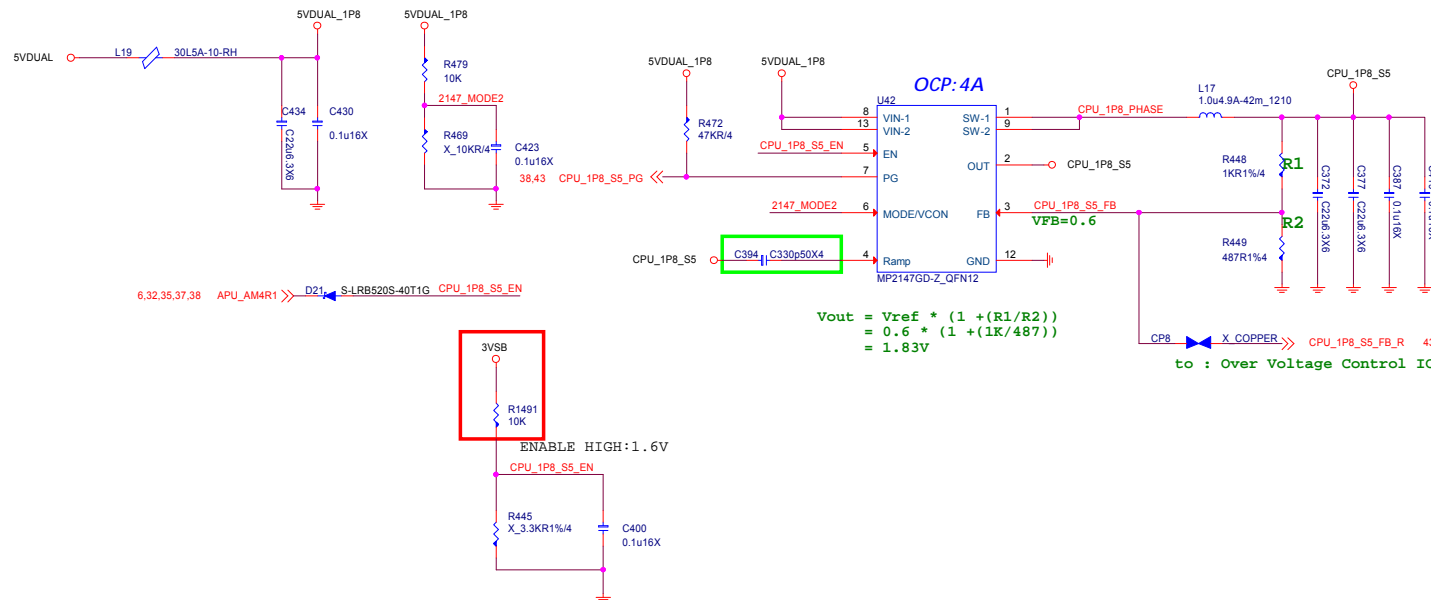


MAX:20.85A

1.2V

0.1uFxl per dimm

 MSI <small>LEARN TO LIVE, LIVE TO LEARN</small>		MICRO-START INT'L CO.,LTD.	
Title DDR PWR VPP25/VT-TP2143			
Size Custom	Document Number MS-7B84		Rev 0A
Date: Friday, February 23, 2018	Sheet 35	of 53	

$$0.5A + 2.0A + 0.9A = 3.4A$$


CPU_VDDP_S0

1.05V/0.9V@S0:8.5A

S0:8.5A

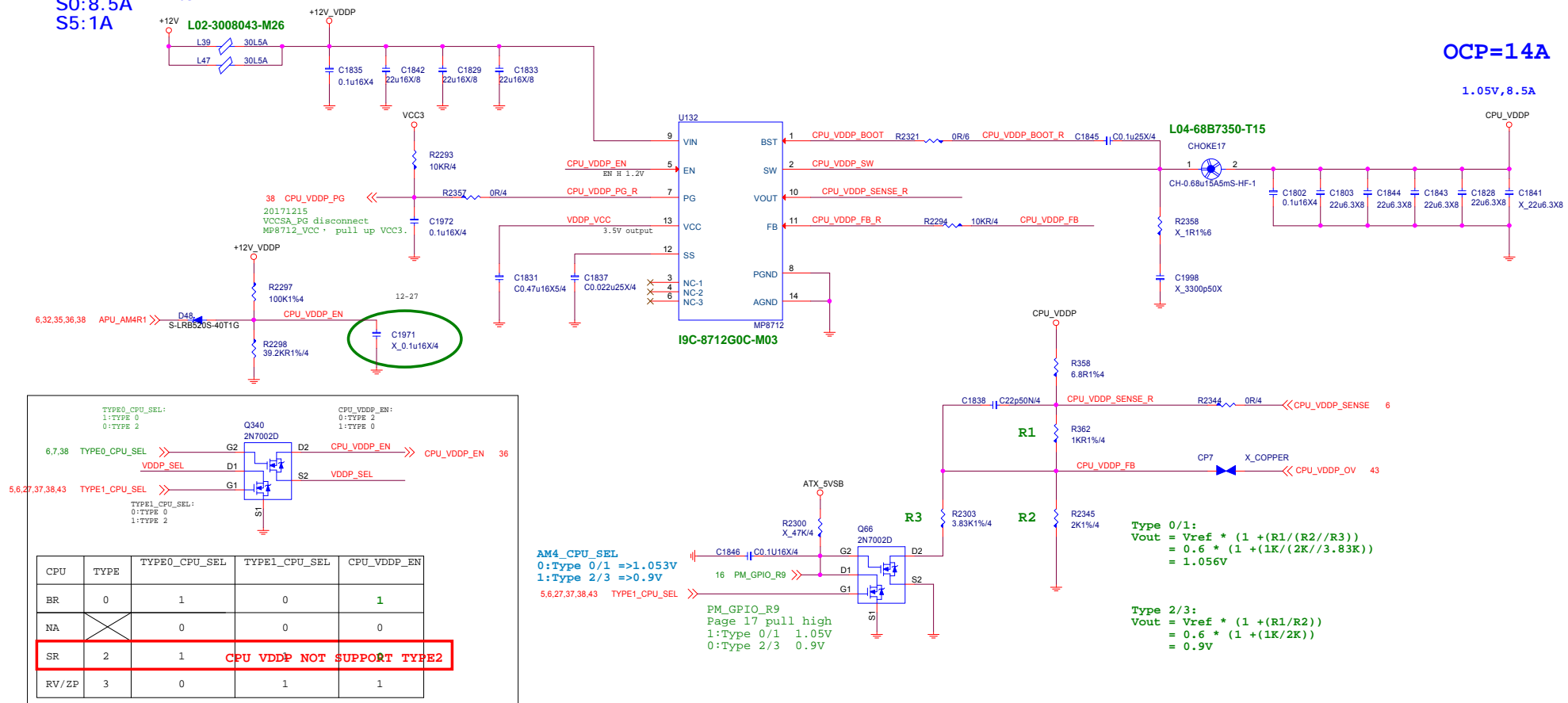
S5:1A

OCP=14A

Input Current= (8.5A*1.05V)/12V/0.8=0.93A

OCP=14A

1.05V, 8.5A



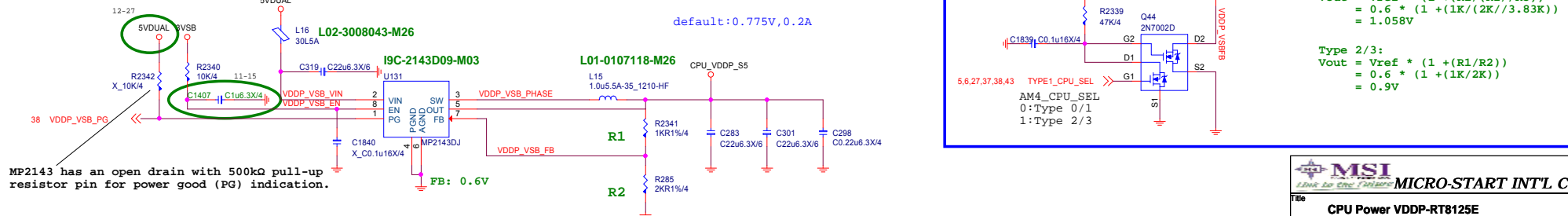
CPU_VDDP_S5

1.05V/0.9V

S5:1A

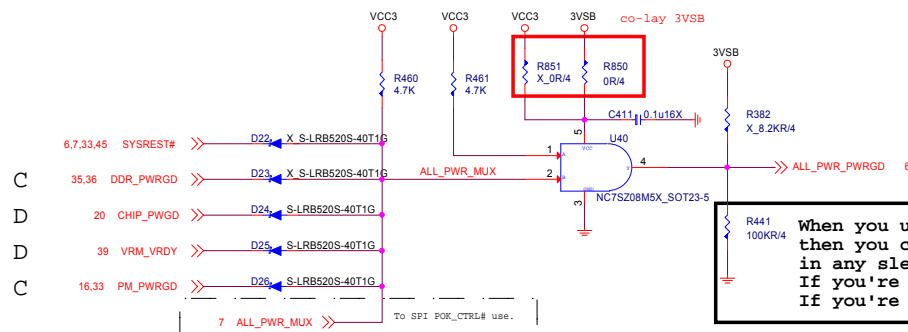
Input Current=0.04A

default:0.775V,0.2A



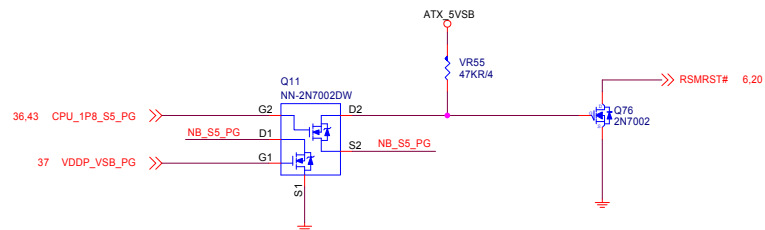
MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

ALL POWER GOOD MUX

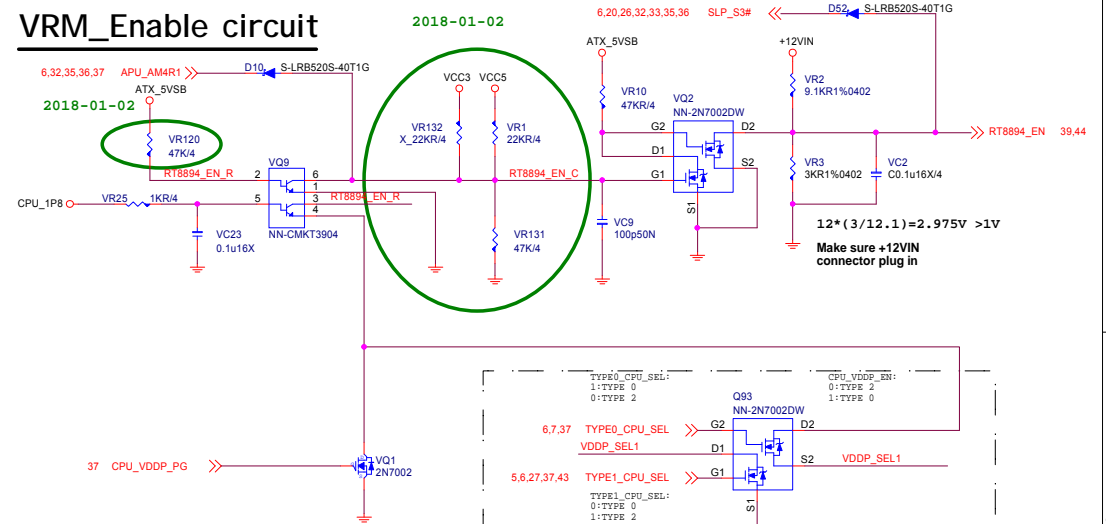


S0 PG

S5 PG



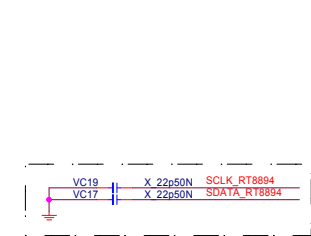
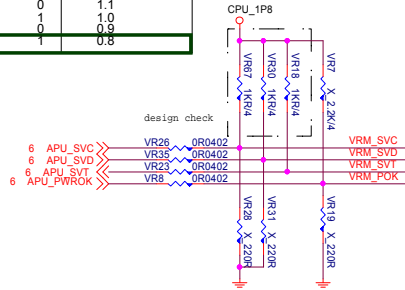
VRM_Enable circuit



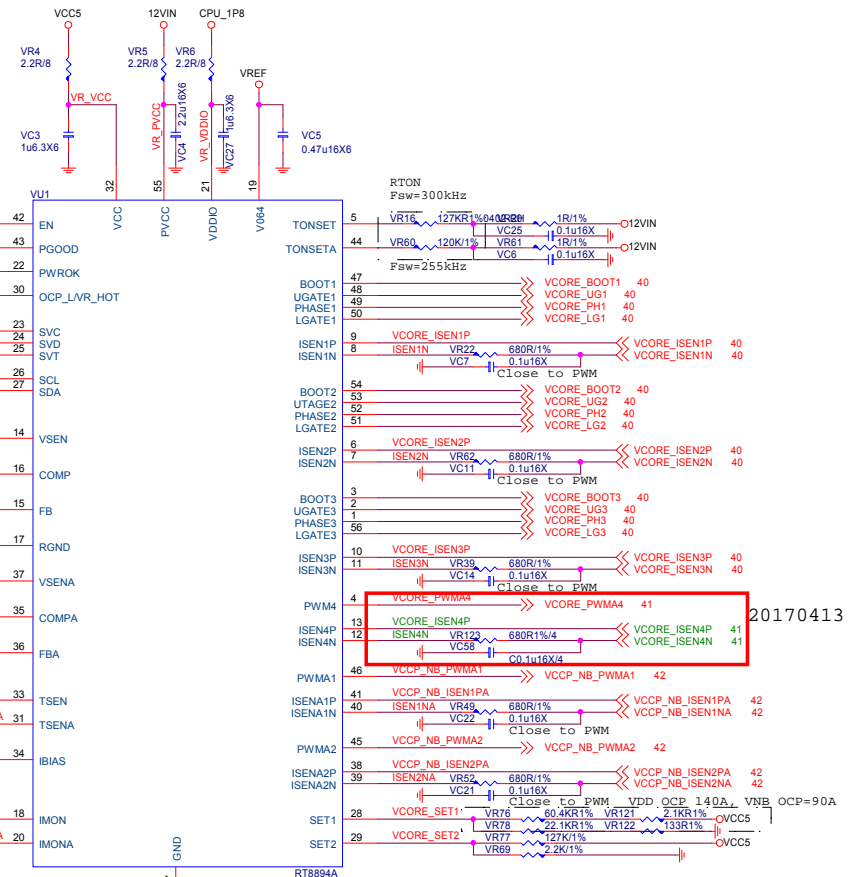
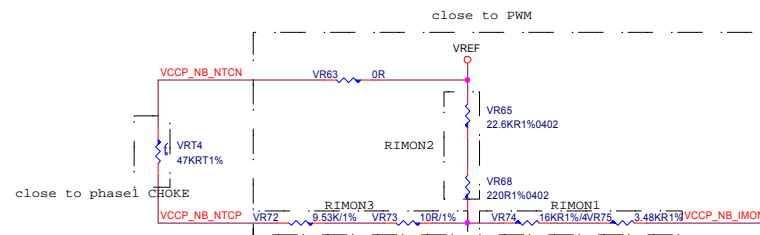
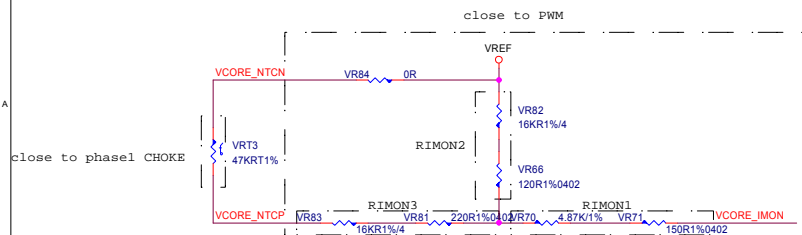
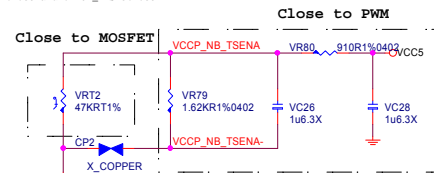
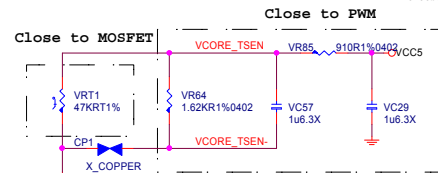
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	0	0	0
SR	2	1	1
RV/ZP	3	1	0

Note:VID Override Circuit

BOOT VOLTAGE		Pre PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



VR_HOT# pull low when T>110°C
VR_HOT# pull high when T drop to 90°C
Choose VRHOT_LOW=51K*VCC and VRHOT_HYS=51K*VCC

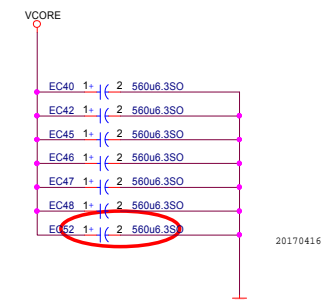
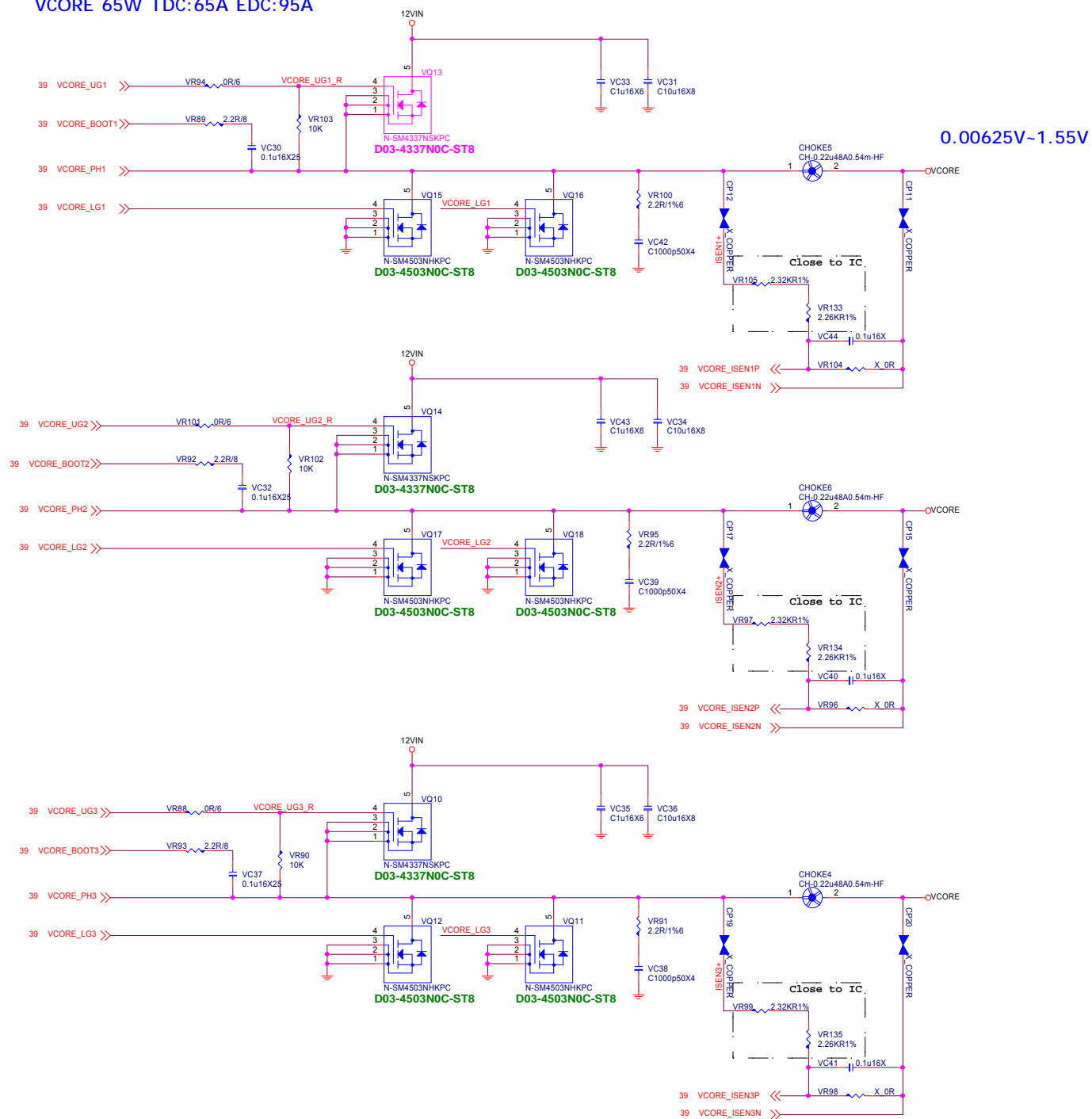


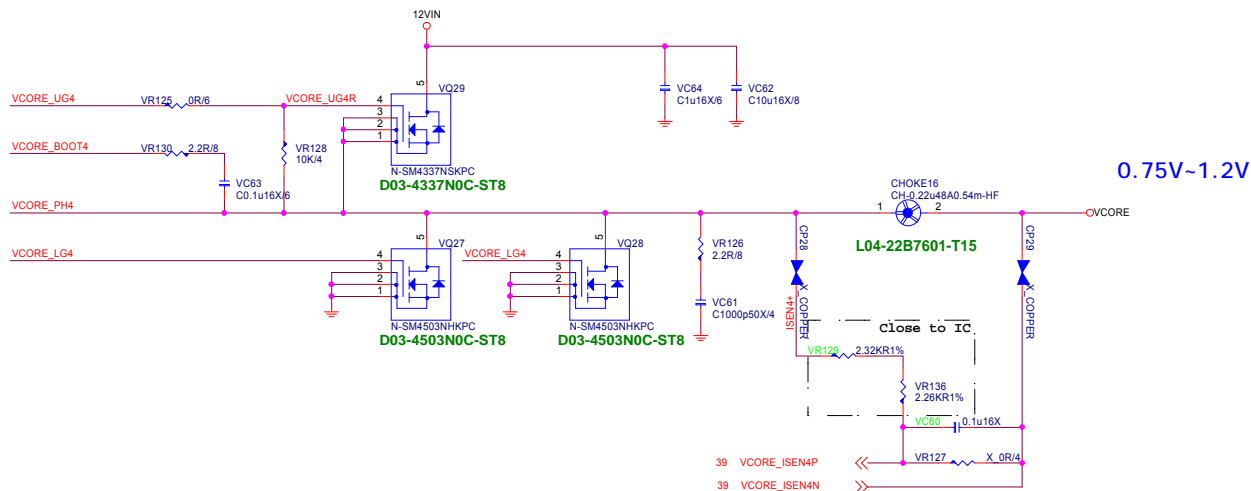
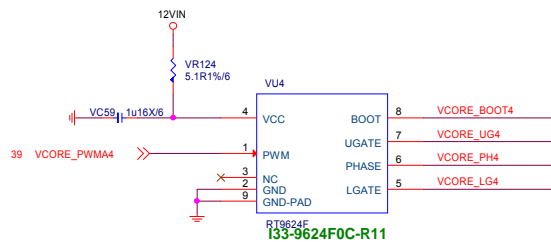
SET1 control ICCMAX,OCP setting
SET2 control internal compensation

SMB Address: 0X40

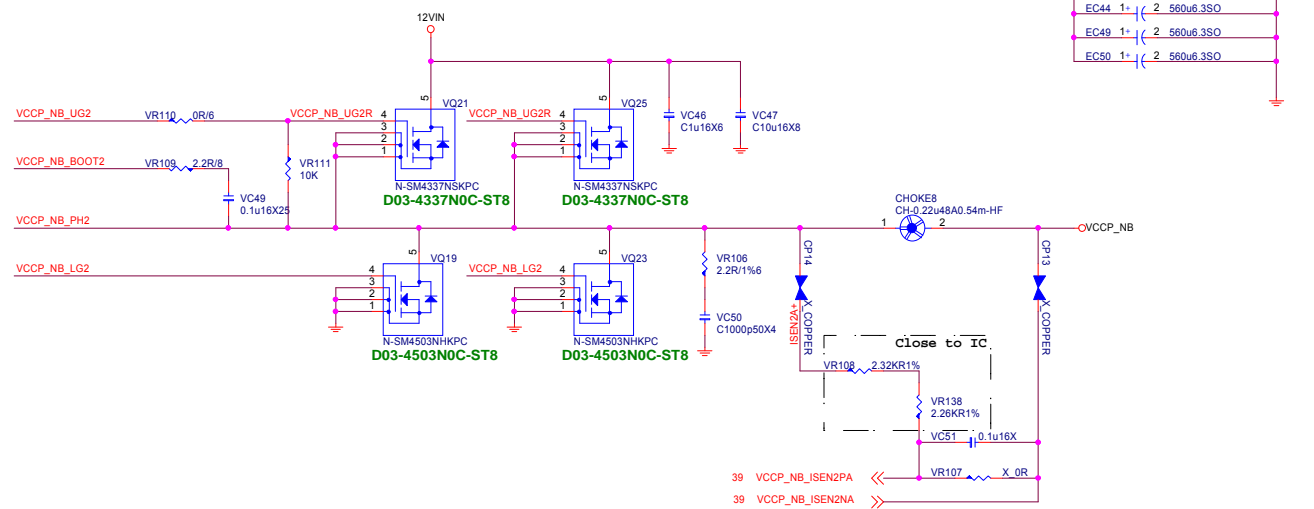
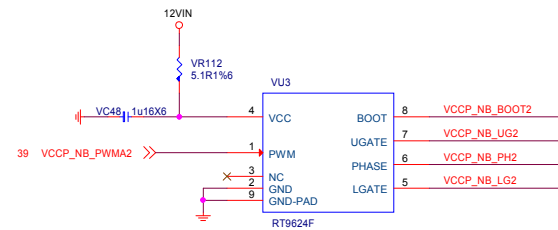
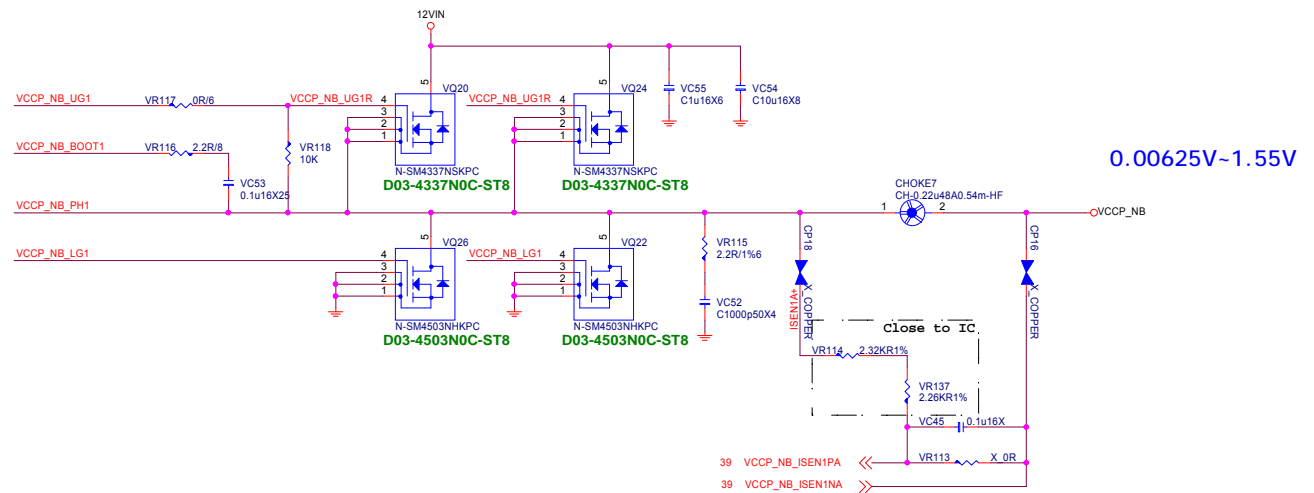
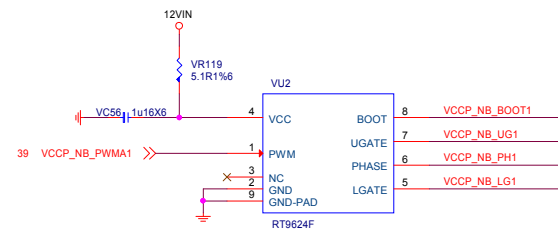
VCORE IccMAX: 125A =>OCP=>140A
VCC_NB IccMAX: 75A =>OCP=> 90A

VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A





VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A



FOR
VCCP_SOC_S5
0.9A

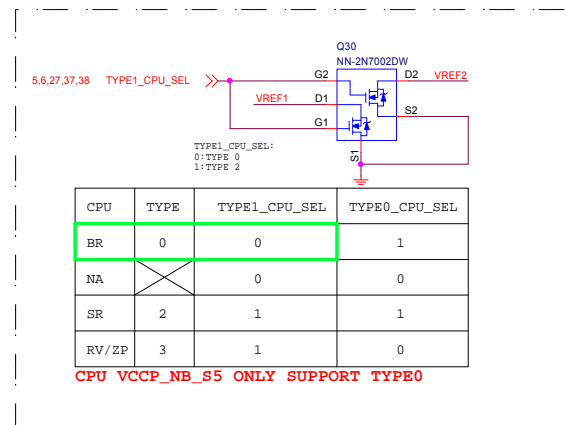
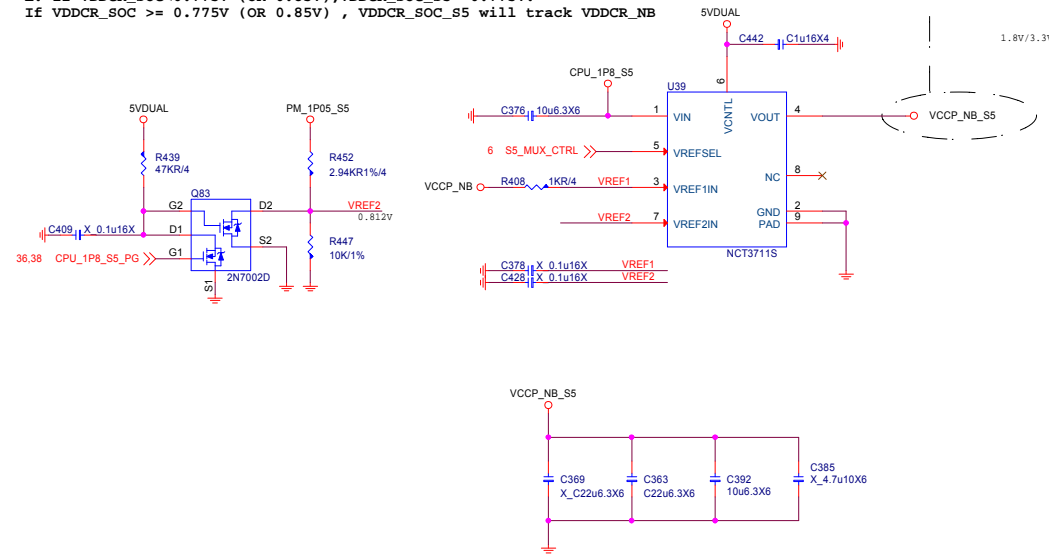
(VDDCR_SOC_S5 is only used for AMD TYPE0)

TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

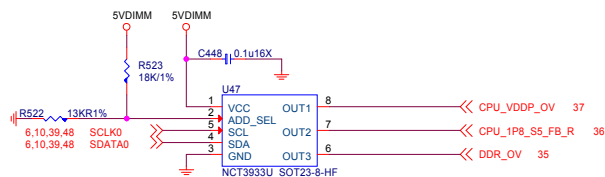
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0

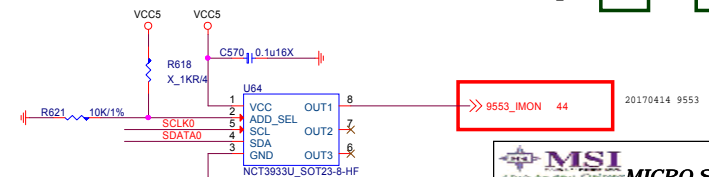


Over Voltage Control IC

0x26:RH=18K,RL=13K



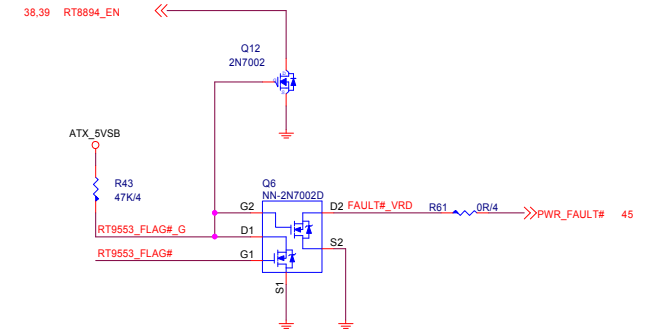
0x2A:RH=OPEN,RL=10K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

NB EDC MAX75A



```
I3933_imon*[(R17*R18)/(R17+R18)]= Istep* RdcR*100
I3933_imon= 10uA/step
Istep=4.785A
```

Close Power Connector

$$= 15.8 \text{ A}$$

EZ Debug LED

VCC5

R227 1KR/4

CPU_LED1 LED04-W-20mA

VCC3

R225 4.7K

6 GPIO97_CPU

Q79 2N7002

6.4 GPIO98_DRAM

Q152 2N7002

R1539 X_GR0402

20170418 update for summit CPU

VCC5

R233 1KR/4

DRAM_LED1 LED04-W-20mA

VCC3

R228 4.7K

6.46 GPIO98_DRAM

R231 X_100KR/4

Q41 2N7002D

VCC5

R236 47KR/4

VGA_LED1 LED04-W-20mA

VCC3

R234 4.7K

6 GPIO99_VGA

Q42 2N7002D

VCC5

R240 1KR/4

BOOT_LED1 LED04-W-20mA

VCC3

R241 4.7K

6 GPIO100_DEVICE

Q45 NN-2N7002D

R248 1KR/4

LED Control by SIO

JLED

2016.07.06 Use TPS25944L

LED GPIO	GPIO097	GPIO098	GPIO099	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

2016.09.13

+12V

C1347
10u16X8

R1232
383KR1%/4

R1233
8.25KR1%/4

R1235
0R0402

R1234
30.9KR1%/4

C1345
C390p50N/4

R1231
26.7KR1%/4

9
10
11
12
13

IN1
IN2
IN3
IN4
IN5

1
14
15
18
19

DMODE
ENULVO
OVP
dV/dt
IMON

16
21

GND
PAD

2016.09.26

12V_LED

C1348
C1u16X

R1222
100KR/4

R1222
475KR/4

R1222
44.2KR1%/4

R980
100KR/4

4
5
6
7
8

OUT1
OUT2
OUT3
OUT4
OUT5

2
3

PGOOD
PGTH

20
17

12V_FLT
ILIM

R1230
24.9KR1%/4

2016.09.13

FADING_LED

R1490
0R0402

Fad LED

Q151
N-PM606BA,SOT23-3

20

FADING_LED

3A

GND_LED

12V_LED

JLED1

H1X4M_BLACK-RH-6

12V_LED

D3
ESD-SFI0402

GND_LED

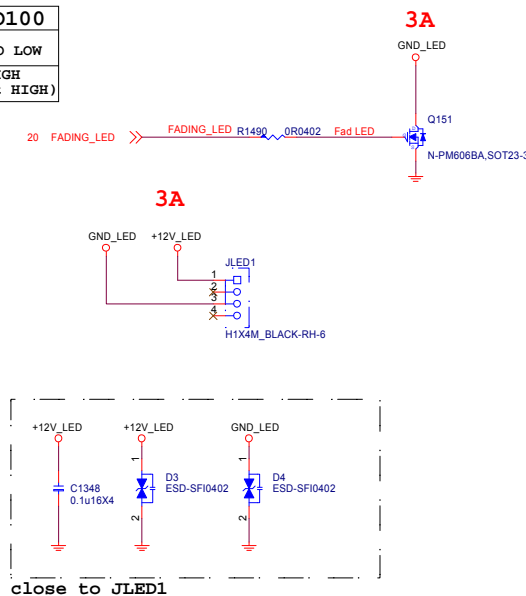
12V_LED

D4
ESD-SFI0402

GND_LED

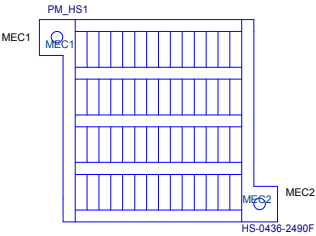
close to JLED1

LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPIO PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

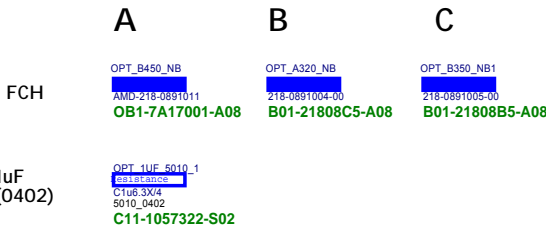


 MSI <small>LIANG DO ENG FABRICATOR</small>		MICRO-START INT'L CO.,LTD.	
Title ALL LED Control			
Size Custom	Document Number MS-7B84		Rev 1.0
Date: Friday, February 23, 2018	1	Sheet 46 of 52	

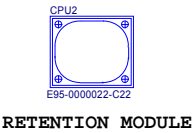
HEAT SINK



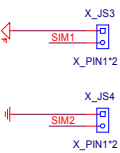
5010 Level



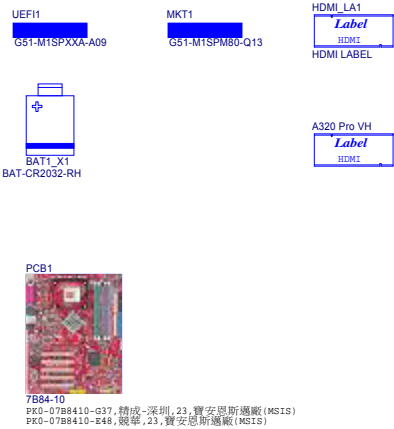
CPU Socket



Simulation

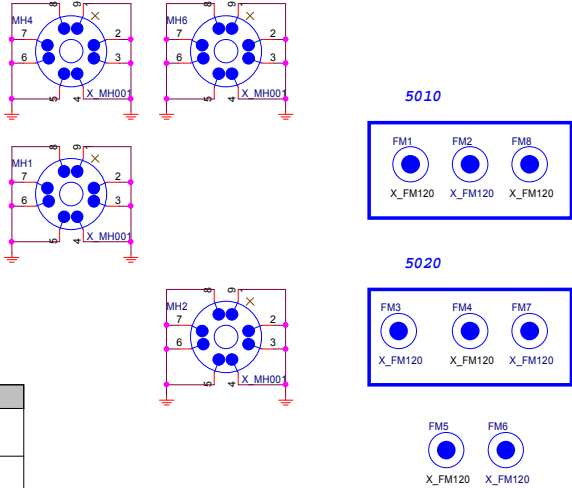


MANUAL PART



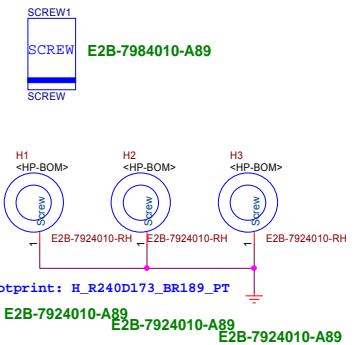
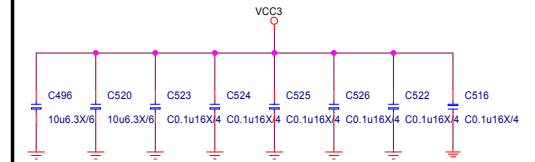
MOS HS(VCORE)

Optics Orientation Holes



OPT	Configure	BOM	Function
		601-7B84-A01	XXXX

3.3V@2.5A



```
TYPE2:  PCIE/SATA
TYPE0:  SATA
```

